DIRC Digital New TDC Reference

March 3, 2004

Philippe Bailly, Jacques Chauveau, Hervé Lebbolo (1), Vanessa Tocut (2),
Alain Vallereau (1)

Introduction :

The DIRC digital new TDC chip is a building block of the DIRC front-end electronics. It receives 16 digital outputs from two 8-channel zero-crossing discriminators (Analog Chip) timed with the single photo-electrons responses of the DIRC detector PMTs. On any Level 1 accept (L1) occurrence, digitized time data associated to this trigger are transferred to a Multi-Event Buffer (MEB) located on a DFB board, and stays until a readout request (Readout Strobe) originated in the central control room and timing system (FCTS) occurs.

1) Requirements :

The DIRC Digital TDC chip has to meet the following requirements :

- 520 ps binning with 250 ps rms precision.

- 34.4 µs full scale.

- 33.6 ns double hit resolution.

- 59.5 MHz reference clock.

- Simultaneous Input and Readout operations.

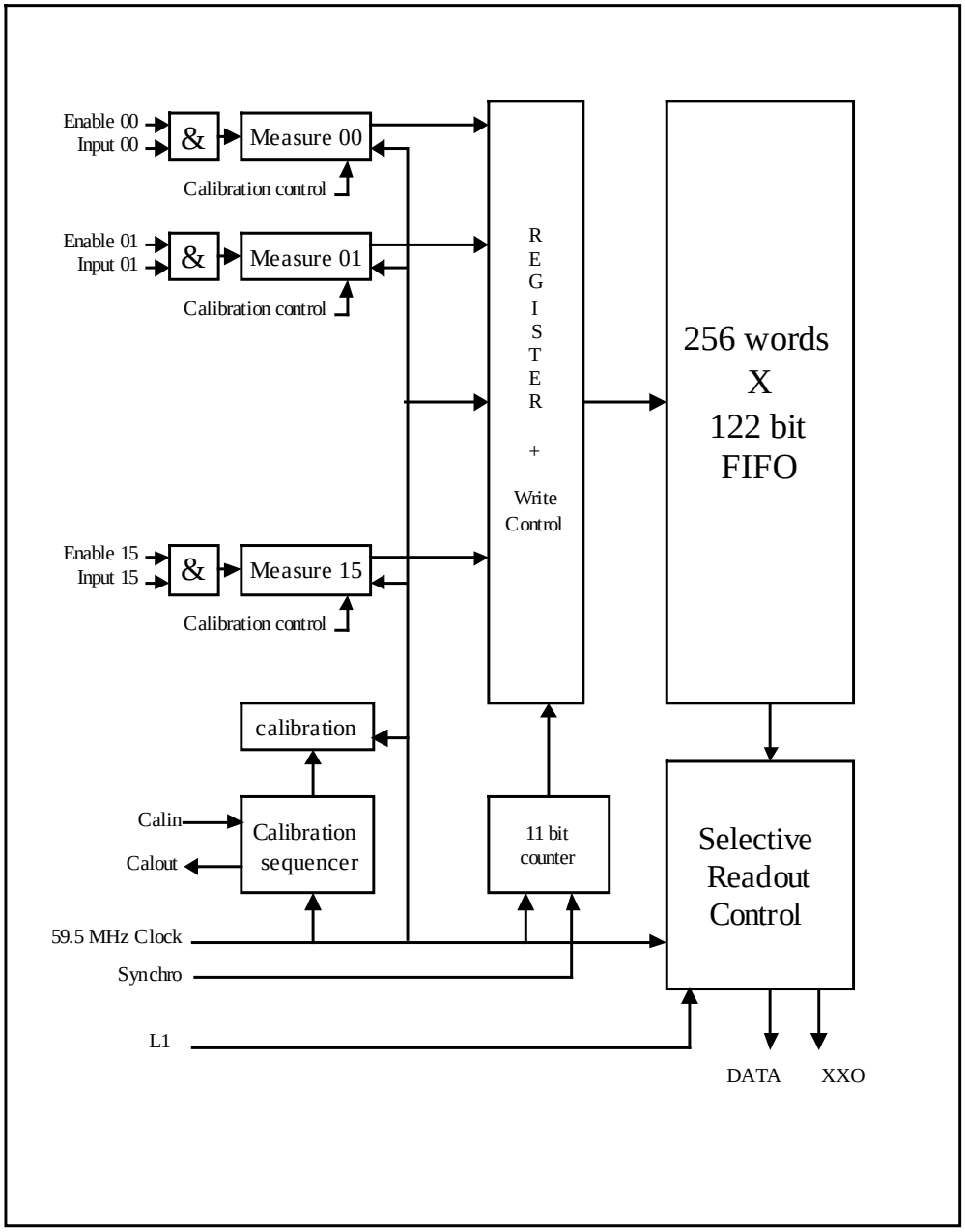
- Selection of data within a programmable time window available at any time for readout.
  - Latency between 64 ns and 16.284 µs (8 bit).
  - Window size (resolution) between 64 ns and 1.984 µs (5 bit).

- Maximum input capability greater than 2 MHz on all channels
  (Latency =10 µs, Resolution =1µs).

- Bit flagging the input capability overloads during the trigger window.

- Maximum number of readout words in one event : programmable, default = 64, with generation of bit flagging the truncature of an event.

(1)Laboratoire de Physique Nucléaire et de Hautes Energies IN2P3/CNRS Paris, France
(2)Laboratoire de l'Accélérateur Linéaire IN2P3/CNRS Orsay, France



DIRC Digital Chip Block Diagram

Figure 1 : TDC block diagram

2) Overall Description :

A block diagram of the chip is shown Fig. 1. Within a 59.5 MHz input clock period, a fine time measurement on 5 bit is achieved using voltage-controlled digital delay lines synchronized on the clock period using a calibration channel generating a reference voltage, to compensate for temperatures, supplies and process variations. This calibration is fully transparent to the TDC operations.
A synchronous counter covers the 11 higher order bit.
One level of buffering in a large FIFO memory (256 words of 122 bit) allow to sort data in time with an incoming trigger, and make them available for readout. This feature allows to reduce by a factor of 10 the amount of data to be read from the DIRC detector. Each FIFO overload during a trigger window is reported at the end of each data block as one bit.

The chip is manufactured by AMS using a 0.6 µm triple metal layer CMOS process.

3) Time Digitization :

The TDC section integrates one 59.5 MHz counter, 16 digital delay lines with 32 taps of 520 ps delay each, a calibration channel made of a delay line identical to the measuring ones, locked on the clock using two analog control voltages stored in the gate capacitors of NMOS transistors controlling the delay of the 32 identical stages, and a time offset.
These analog control voltages are common to all channels assuming a good process uniformity within the chip, measured on previous TDC chips designs using the same technology.
An incoming signal latches the counter state in a 11 bit register, and propagates in the delay line. The next clock positive edge latches the state of the delay line in a 32 bit register, the result being binary encoded to five bit. Finally the 10 most significant bit of the counter are written into the FIFO as coarse time and the least significant bit and the 5 encoded bit are written in the FIFO as fine time for each channel. This allows the minimum period of writing in the FIFO to be 32 ns instead of 16 ns.

The delay lines, the synchronous mechanism between the clock and the inputs, the charge pump used as phase feedback have been implemented as custom designs, at transistor level.
A state machine sequences the calibration process that can be activated using an input pin (Calin). The end of that process which takes a few microseconds in total, activates an output signal (Calout). Calibration has been found stable for minutes, allowing to keep the chip free of any other switching than the necessary measurements, giving the best linearity results.

4) Selective Readout :

A block diagram of the selective readout is shown in Fig. 2. The TDC is sensitive to any positive edge applied to the inputs. Data (11 bit counter + 5 bit delay line) are stored in a temporary register. As the double pulse resolution is 2 clock period, data are transferred at the maximum speed of half the clock frequency in a big FIFO memory containing 256 words of 122 bit arranged as follow :

16 bit : fired channels.
10 most significant counter bit.
16 * 6 bit : least significant counter bit , 5 delay line bit.

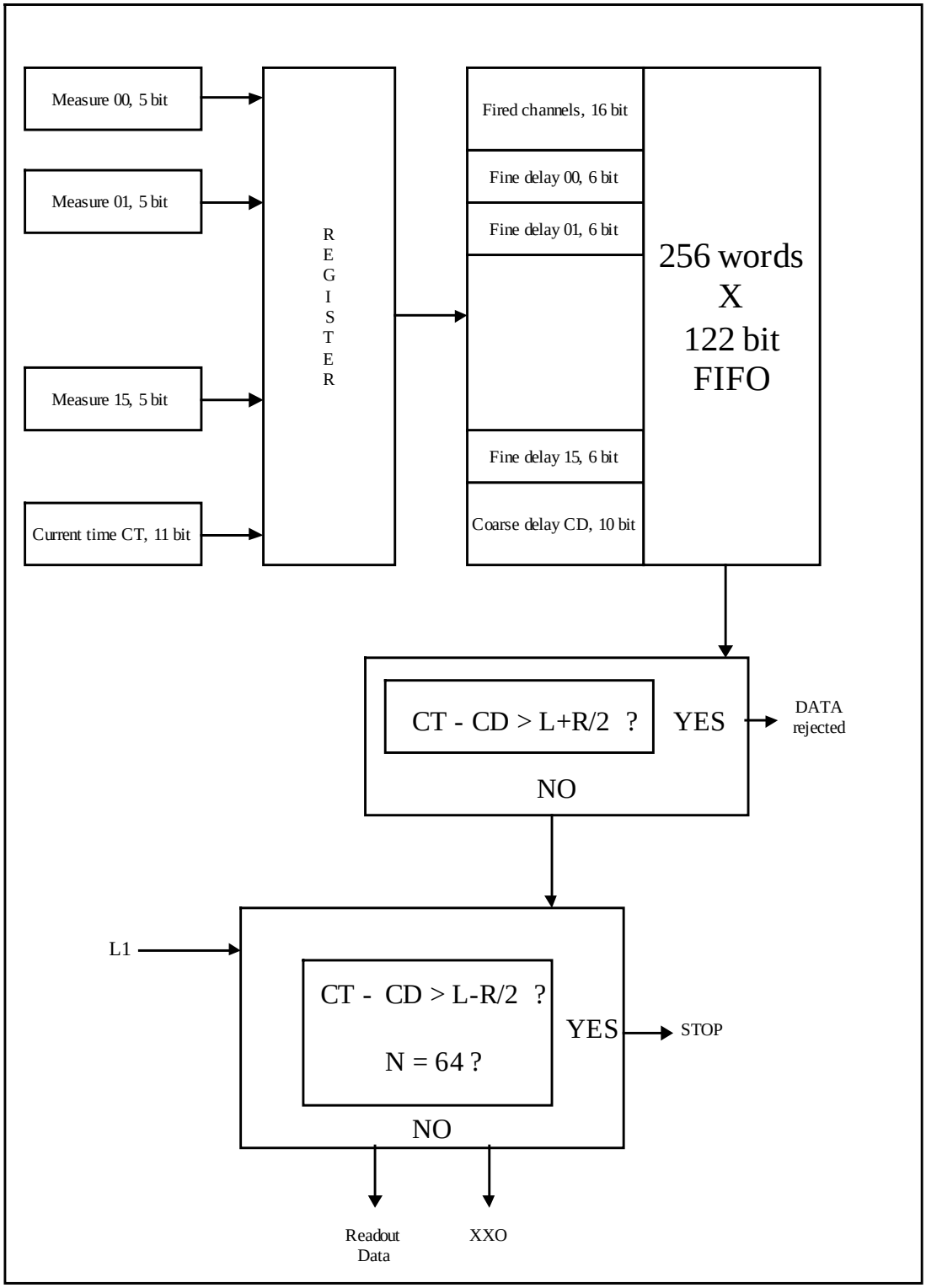


Figure 2 : Selective Readout process block diagram

At this stage, a control is continuously done on the first available data at the output of the FIFO to see if it is too old, in this case data is rejected and next one is present at the output of the FIFO.

When a L1 accept occurs :

1)The counter state is latched as L1 time and readout in the first word (header of the event)

2)Data available is tested to see if it is too young, if it this case the last word of the event (trailer) is readout. If not, data is readout and next one is present at the output of the FIFO. Process is repeated until data is too young or number of data transferred is greater than 63, in this case transfer is stopped, trailer is sent when a bit flagging the truncature of the event.

The readout process is sequenced at half the master clock (30 MHz) and can be managed within the time before another L1 accept comes (2 ?s). When data are readout, the selective readout process filling the FIFO is still working, minimizing the dead-time.
If input occurs when FIFO is full, nothing is written in the FIFO, the FIFO-full bit is set and will be readout with the associated event, indicating data have been lost.

5) Registers :

Three registers are used to control the device.

- Latency and Resolution register.
- Channel enabling.
- Maximum number of words in one event (default = 64).

All registers can be read back.

6) I/Os Description :

S<15:0> : 16 independent Start TTL inputs.
Any positive pulse of more than 5 ns duration applied to these pins result in a time digitization of the rising edge with respect to the next positive edge clock.

Bs<1:0> : 2 TTL inputs.
These bits, combined with D<21:20> as input, select the function of the multiplexed inputs/outputs D<21 :00>. This 22 bit port is used for data access, register read and write, test input and output as follow :

Bs = 00, D<21:00> configured as output.
Bs = 01, D<21:00> paralleled access for register read or write.
Bs = 10, D<21:00> tests, and paralleled access for register read or write.

D<15:0> : 16 inputs/outputs TTL in CMOS out.

Bs = 00, Output data.
Bs = 01, Parallel access bus for register read and write.
Bs = 10, Test data output.

D<19:16> : 4 CMOS output.

Bs = 00, Output data.
Bs = 10, Test data output.

D<21:20> : 2 inputs/outputs TTL in, CMOS out.

Bs = 01, 16 bit Register read and write operation.

D<21:20> = 00,

Trigger latency and resolution, L+R/2 8bit <07:00>

L-R/2 8bit <15:08>

D<21:20> = 10, Channel enable register <15:00>

Bs = 10 & D<21:20> = 01, number of clock period of the event transfer. <08:00>

CK : TTL clock input.

Rw : TTL input. Write register control.

Rw = 0, write operation. Rw = 1, read operation.

Strb : TTL input. Strobe for registers access. Active low.

Write : Data should be stable at least half a clock period before strobe positive edge, maintained half a clock period afterwards.

Read : Data is enabled at least half a clock period after strobe negative edge.

L1 : TTL input. First level trigger accept input. Active high.

This input has to be synchronous with the clock negative edge, and maintained high for one clock period. Trigger time associated to that period is internally latched one the clock leading edge . See Fig. 3.

Data falling in the selected time window are output at half the frequency of the clock.

Sync : TTL input. Clear time counter. Active low.

Clock synchronous, active during one clock period. Counter is cleared on the clock falling edge. After a Sync signal data in the FIFO are not relevant before at least a latency delay.

Cs : TTL input. Chip Select. Active low.

When high output buffers are in high impedance state.

Res0 : TTL input. Clear FIFO. Active low.

Reset the content of the FIFO.

Res1 : TTL input. Reset. Active low

General reset, including registers.

C1 : TTL input. Calibration input. Active low.

Bs = 00, Calibration input. Triggers a calibration cycle.

Co : CMOS output, Calibration output.

Flags a successfully calibration cycle termination.

Xxo : CMOS output. Strobe for output data

Bs = 00 : Strobe for output data, data to be latched on rising edge. See Fig. 3.

Eight Vdd pins (5 volts).
Nine Ground pins

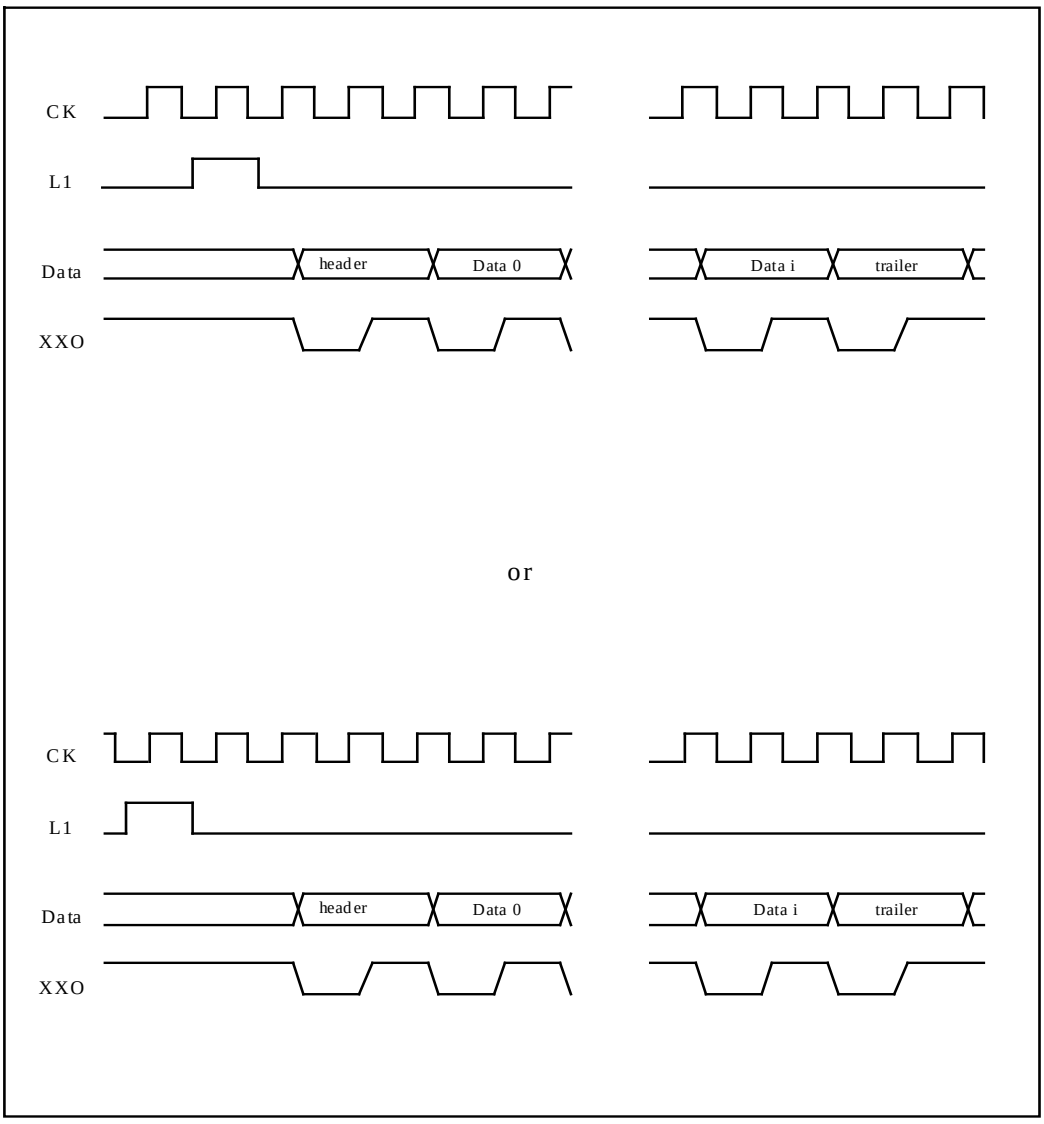


Figure 3 : Digital TDC Chip Readout Sequence

7) Data packet structure :

Two MSB indicate whether the word is a header, data or a trailer of the event.

Header : 10, nine 0, 11 bit trigger time (MSB left).
[10000000000xxxxxxxxxxx]

Data : 00, four channel address bit MSB left, sixteen time bit MSB left.
[01aaaaxxxxxxxxxxxxxxxx]

Trailer : 11, two 0, FIFO overload bit, truncature bit, sixteen 0.
[1100OT0000000000000000]

8) Tests Benches :

All chips have been tested in the lab using the following test bench :

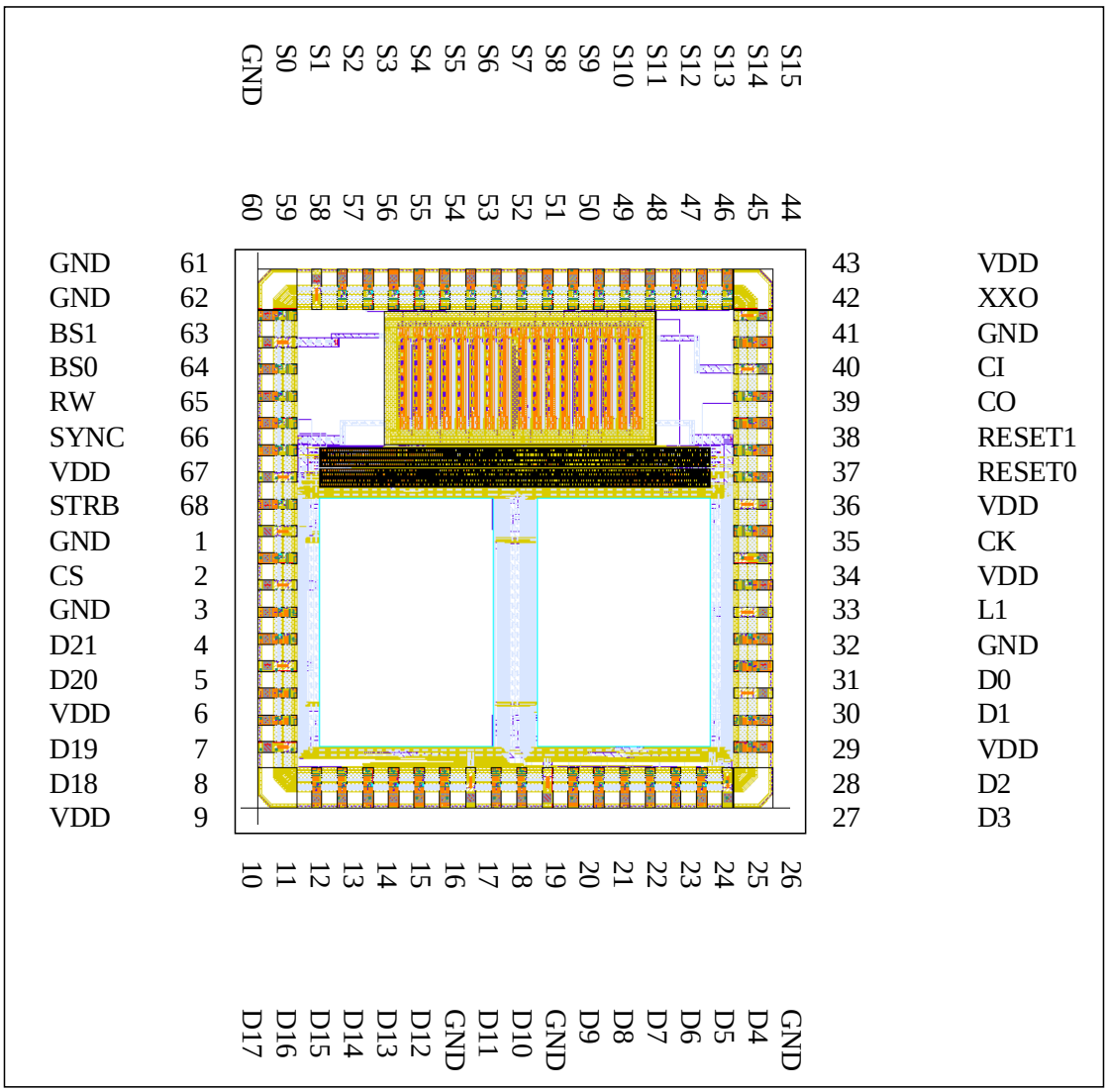
- A dedicated 4 layers printed circuit board.
- A precision 9210 LeCroy IEEE 488 programmable pulse generator.
- A precision 81110A Agilent IEEE 488 programmable pattern/pulse generator.
- A PS5010 Tektronix IEEE 488 programmable low voltage power supply.
- A personnel computer running LabView acquisition program.
- A National Instruments digital I/O interface.

The key measurements are :

- Locking range,
- Linearity within one clock period,
- Linearity over several clock period,
- Selective readout with simultaneous inputs and read,
- Input capability,
- Data packet generation,
- Crosstalk,
- Power.

9) Package :

The DIRC TDC chip is available in 68 pins PLCC package.


GND 61
GND 62
BS1 63
BS0 64
RW 65
SYNC 66
VDD 67
STRB 68
GND 1
CS 2
GND 3
D21 4
D20 5
VDD 6
D19 7
D18 8
VDD 9
43 VDD
42 XXO
41 GND
40 CI
39 CO
38 RESET1
37 RESET0
36 VDD
35 CK
34 VDD
33 L1
32 GND
31 D0
30 D1
29 VDD
28 D2
27 D3
60 GND
59 S0
58 S1
57 S2
56 S3
55 S4
54 S5
53 S6
52 S7
51 S8
50 S9
49 S10
48 S11
47 S12
46 S13
45 S14
44 S15
10 D17
11 D16
12 D15
13 D14
14 D13
15 D12
16 GND
17 D11
18 D10
19 GND
20 D9
21 D8
22 D7
23 D6
24 D5
25 D4
26 GND