Tens Picosenconds Digital ASIC Time To Digital Converter for Phisics Experiments

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LPNHE, Electronics group 9/03/2012

Outline

- Why a time measure?
- Different TDCs
- The TEMPO TDC
- A first version @ 180nm
- The final chip @ 90nm

Why a time measure?

Time To Digital Converters (TDC) are widely used in many different fields

Physics experiments

- Time Of Flight
- Positron Emission Tomography (PET)
- Laser applications

…

Applied Electronics

- All digital frequency synthesis
- GFSK transceivers (frequency modulators)
- On chip test structures

…

All Digital TDC

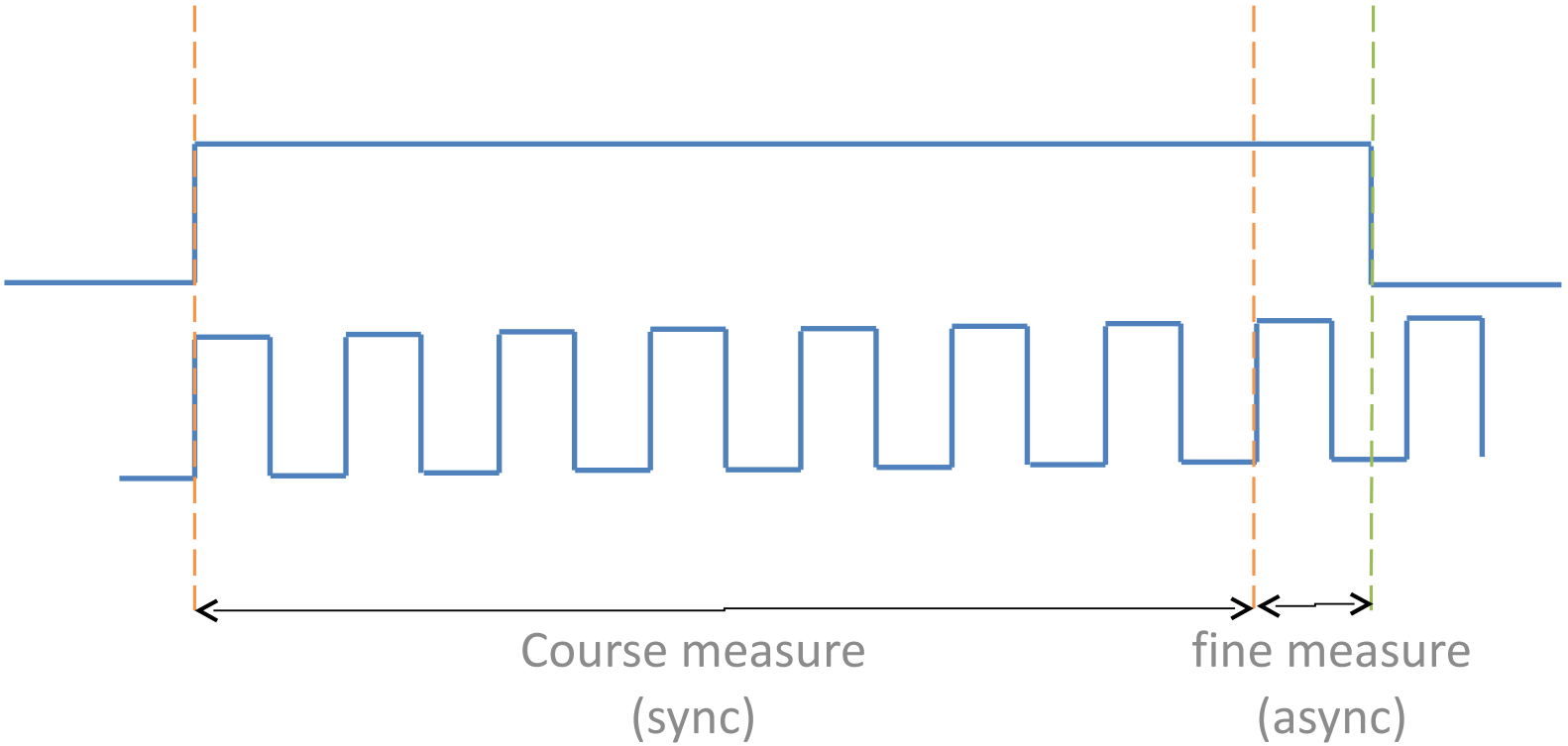
Many different schemes to implement a TDC (both analogic and digital)

Digital Scheme

- More performances on Avaliable Technologies
- Easy to port design in different tech
- Performances scale almost linearly with tech

How to design a TDC

To have a good resolution on a wide dynamic range a synchronous counter and asynchronous fine interpolator are realized

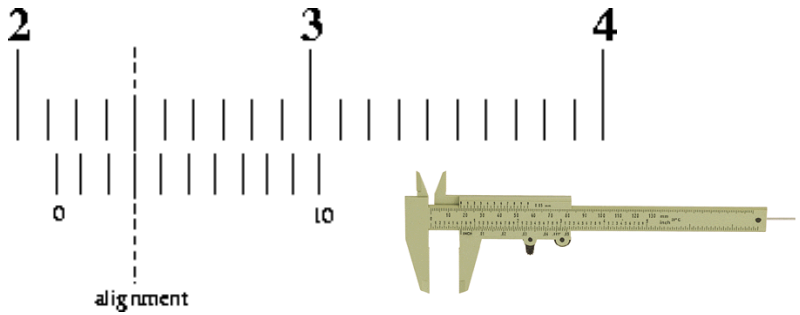


The fine measure

There are many different schemes to design the fine interpolator

Vernier Based

The time interval is compared to a fixed time scale (like a caliper)

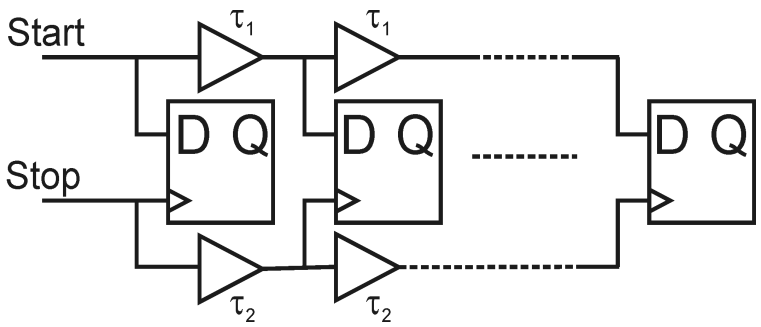


Direct Measure

The time interval in measured in terms of a fixed quantity (like a meter)

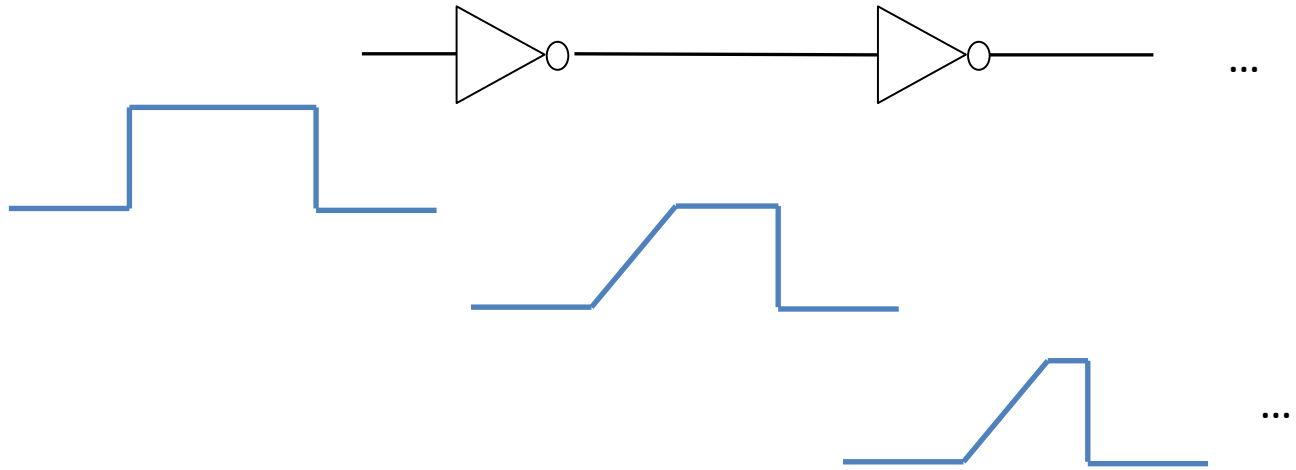
Vernier Based design examples

$\tau 2 \neq \tau 1$

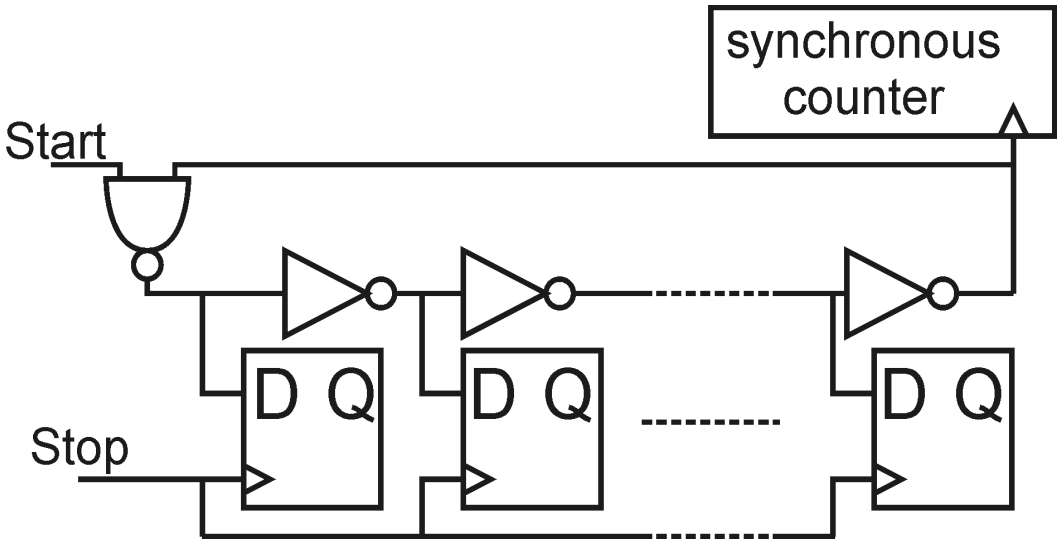


Resolution is $|\tau 2-\tau 1|$

TLtH ≠ THtL



Direct Measure design

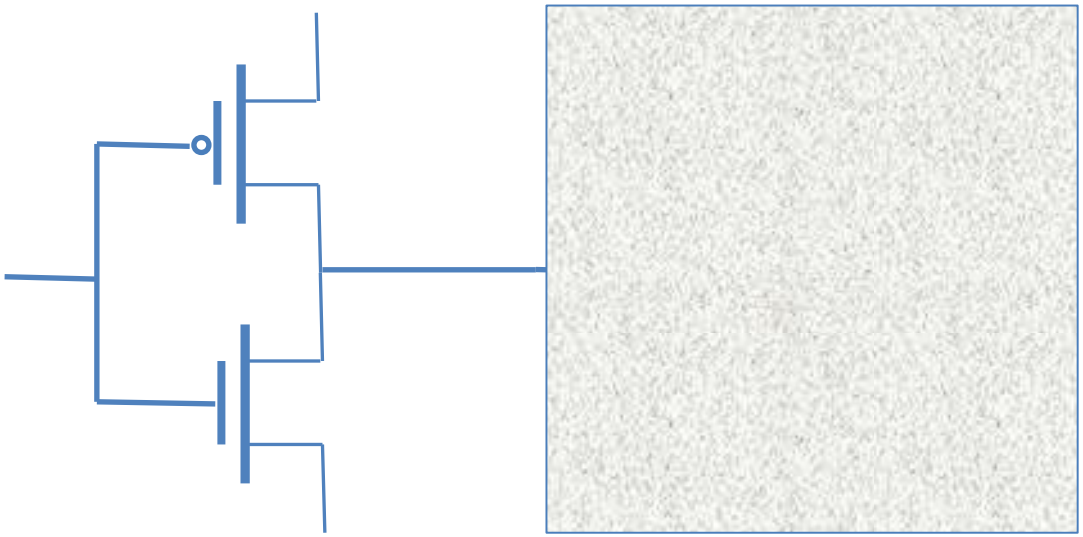


Resolution = tinv

Which inverter?

In a direct measure scheme the inverter design is the key element to achieve a good resolution

CMOS inverter (static)

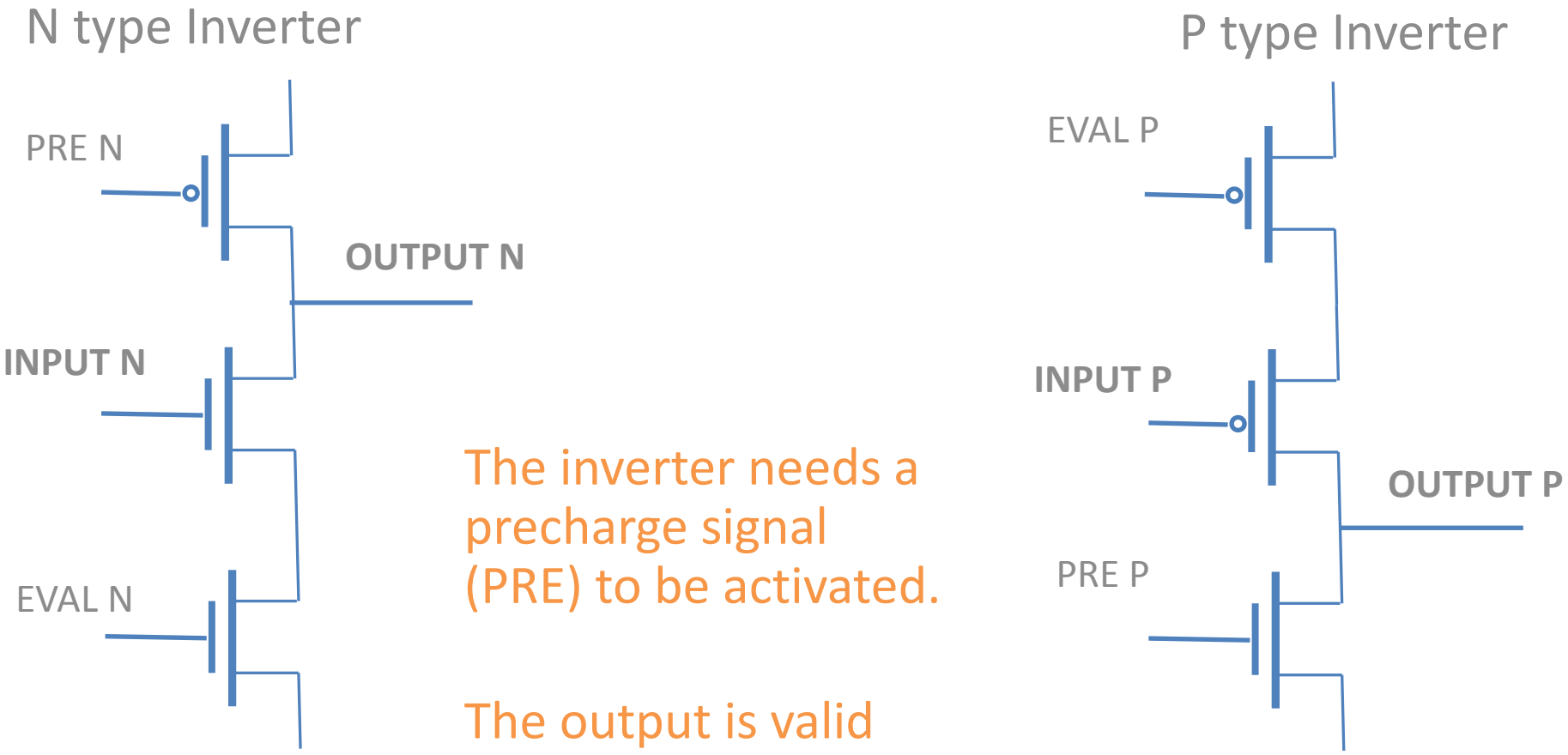


The inverter delay optimization is a tradeoff between:

- MOS dimensions
- parasitic C
- rise fall time

Which inverter?

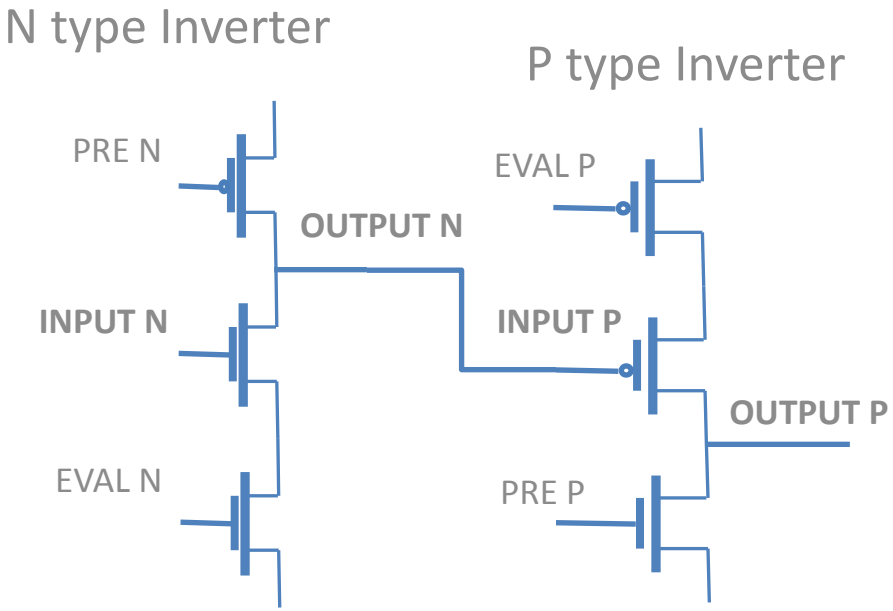
NORA inverter (dynamic)



The inverter needs a precharge signal (PRE) to be activated.

The output is valid after the signal EVAL

NORA Logic
pros & cons



PRO

- speed (Eval parasites are not on the signal path)
- TH2L ≠ TL2H

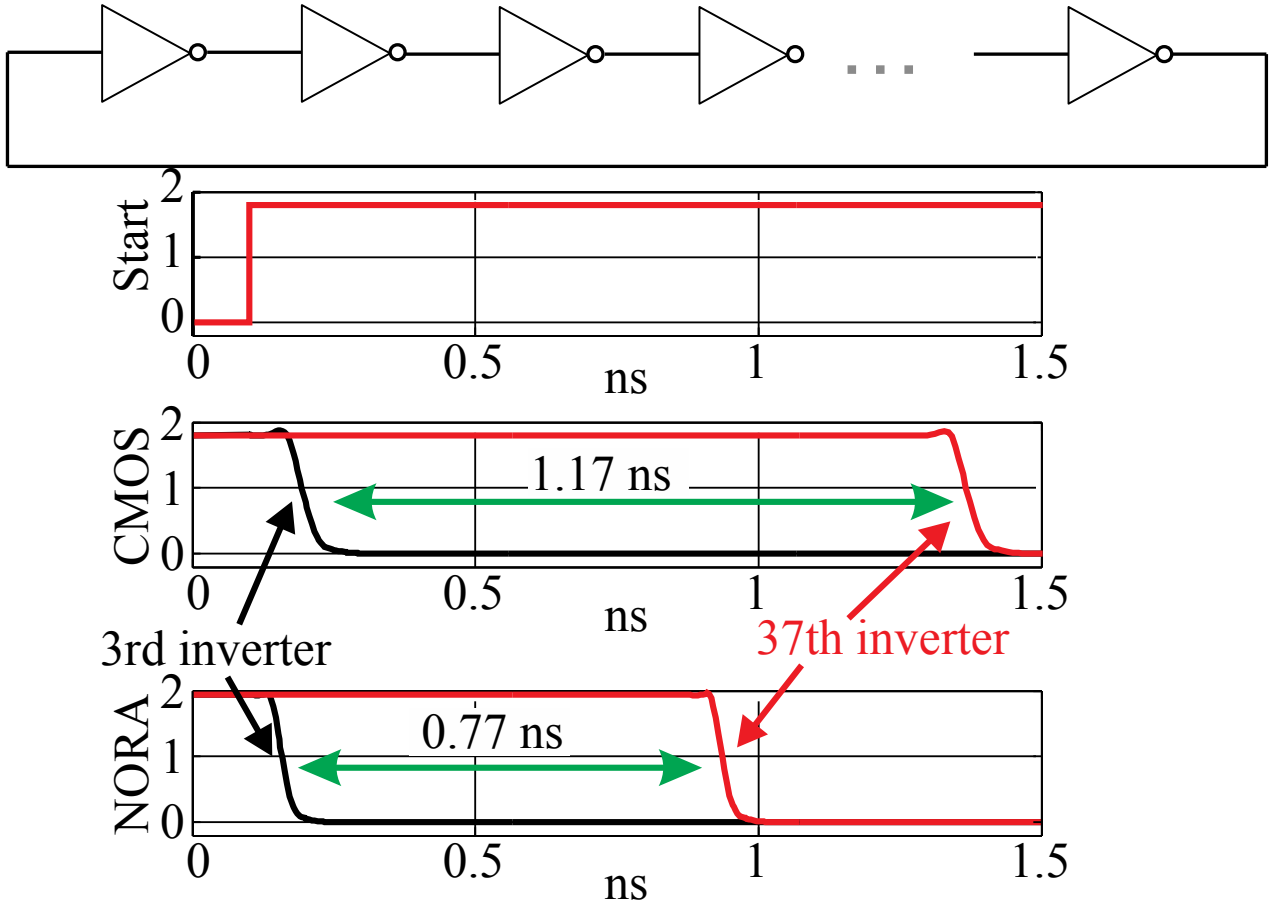
CONs

- Many signals
- TH2L ≠ TL2H

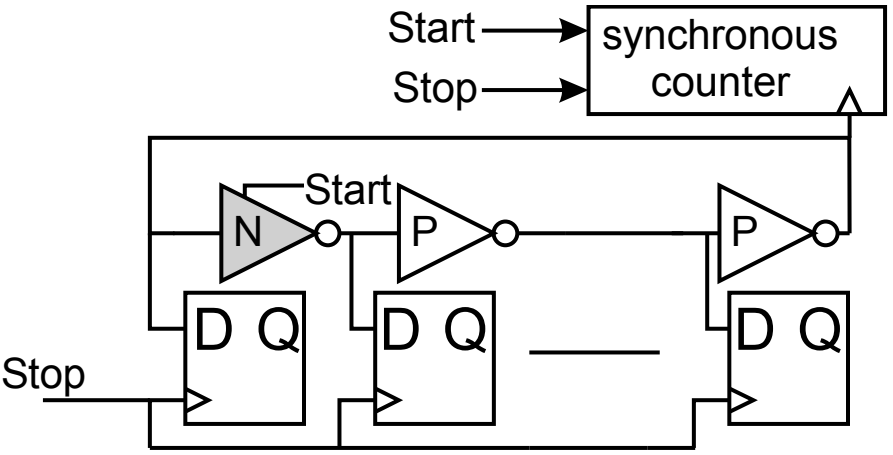
NORA vs. CMOS

To evaluate the performances a comparative simulations was performed @ 180nm

NORA is 34% Faster than CMOS

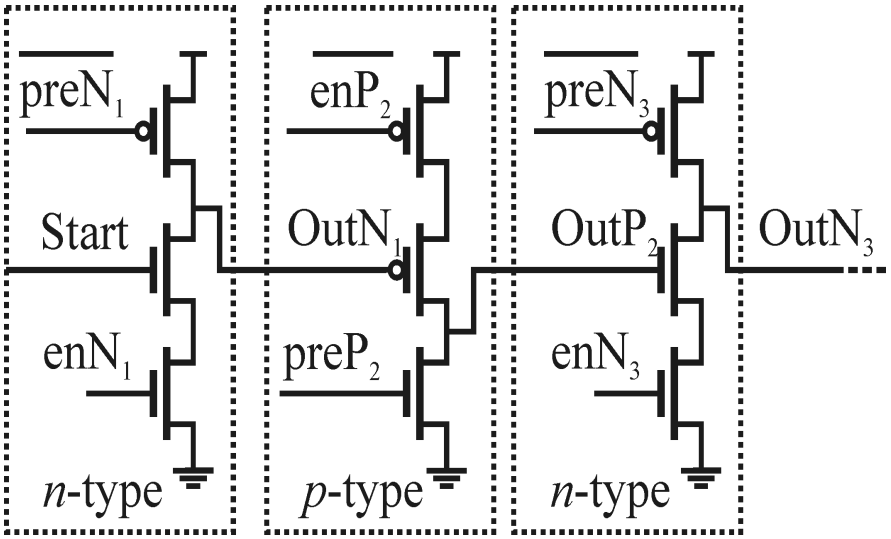


The TEMPO scheme

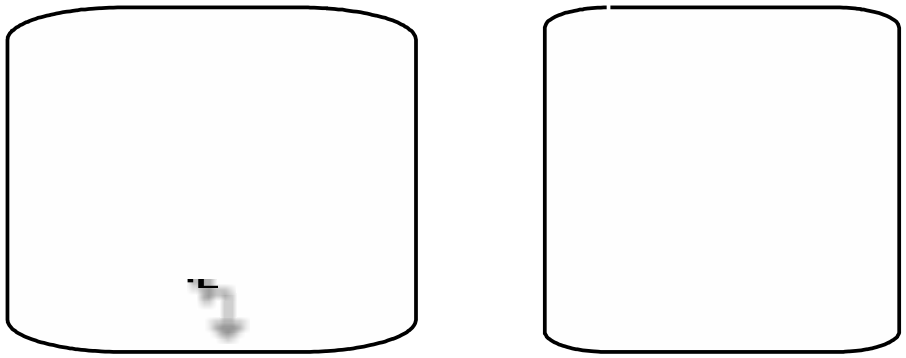


- High resolution
- Reduced dead time
- Low power

Inverters in the fine interpolator are designed using NORA logic

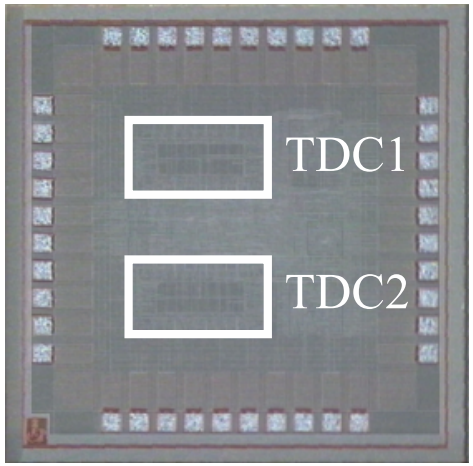


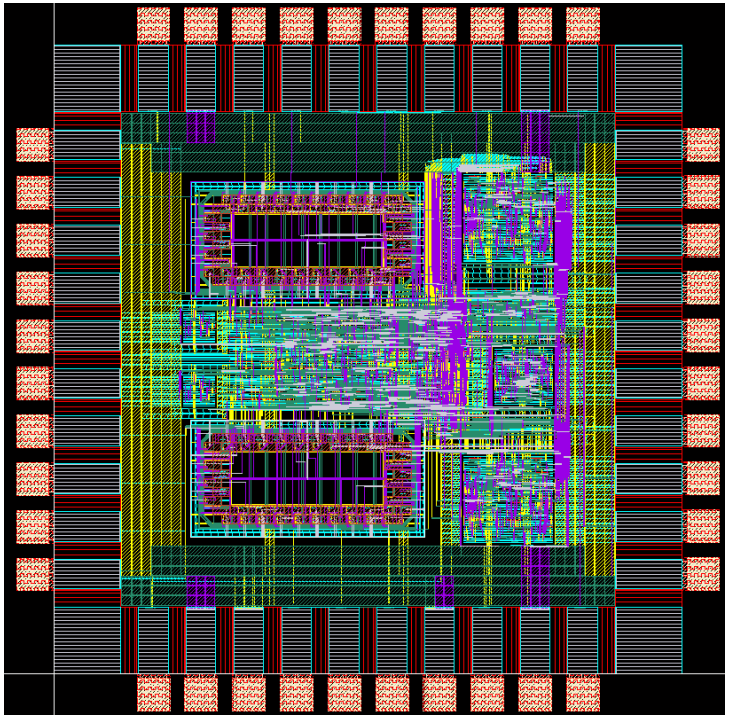
The TEMPO scheme



A first chip @ 180nm (UMC)

To validate our scheme a first version was realized



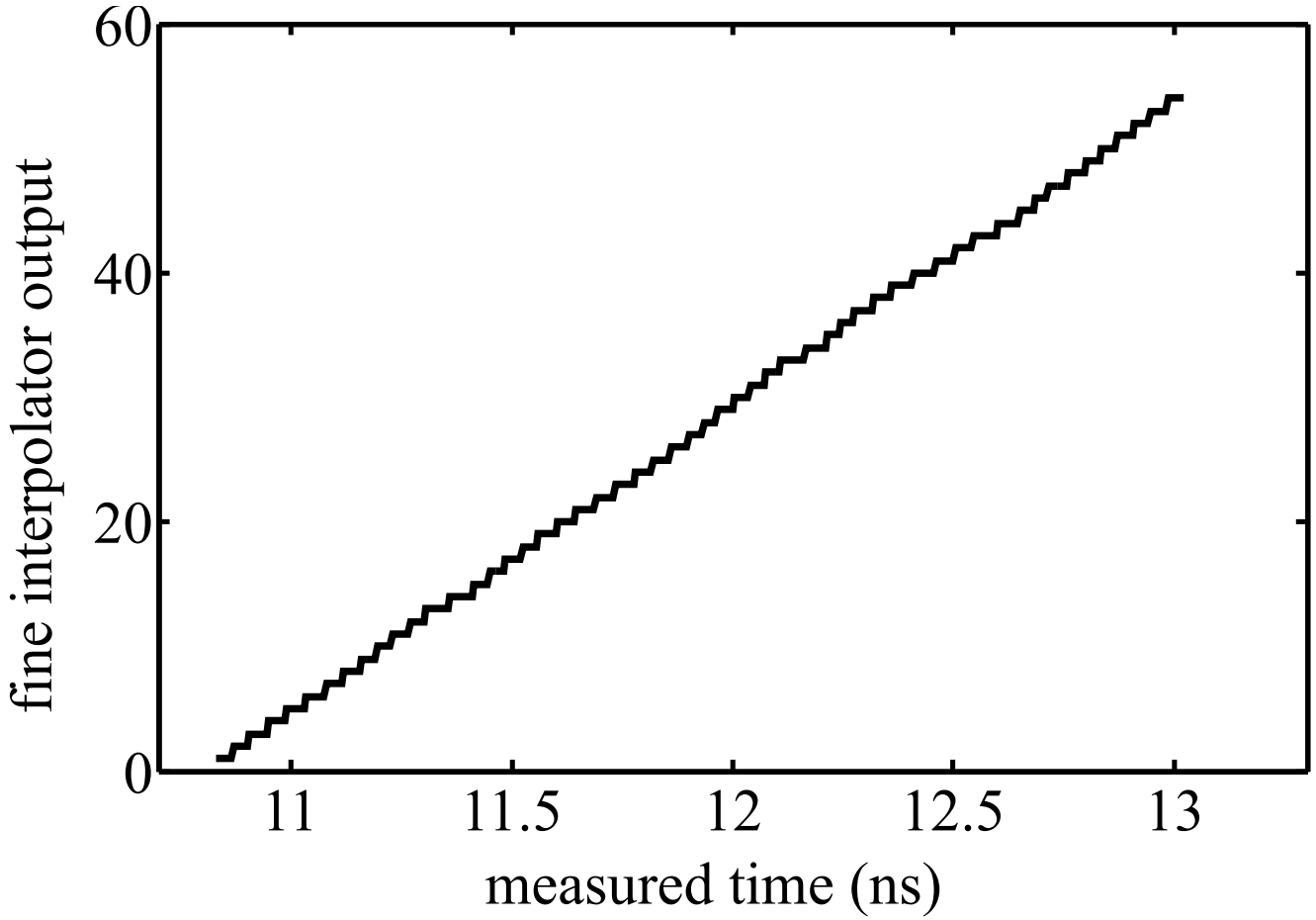


Full custom design for delay lines

TDC1 measure the time between START & Stop

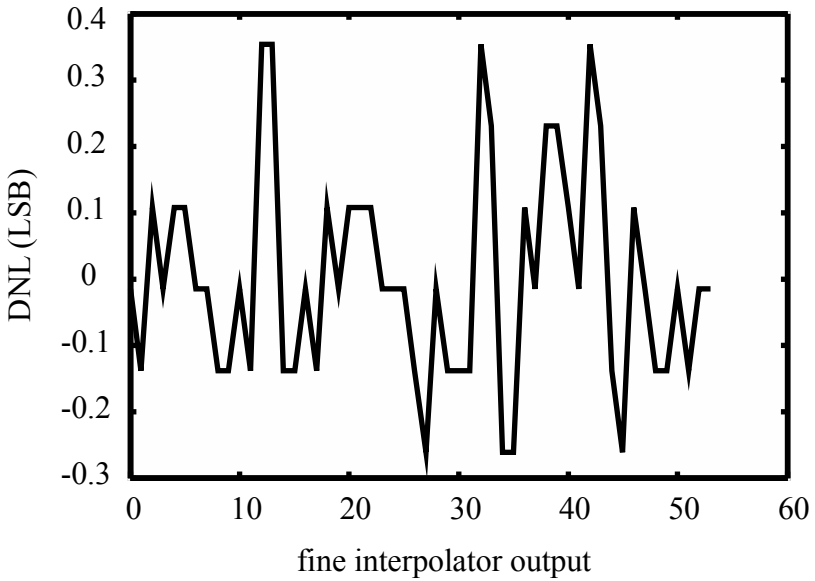
TDC2 measure a clock period (calibration)

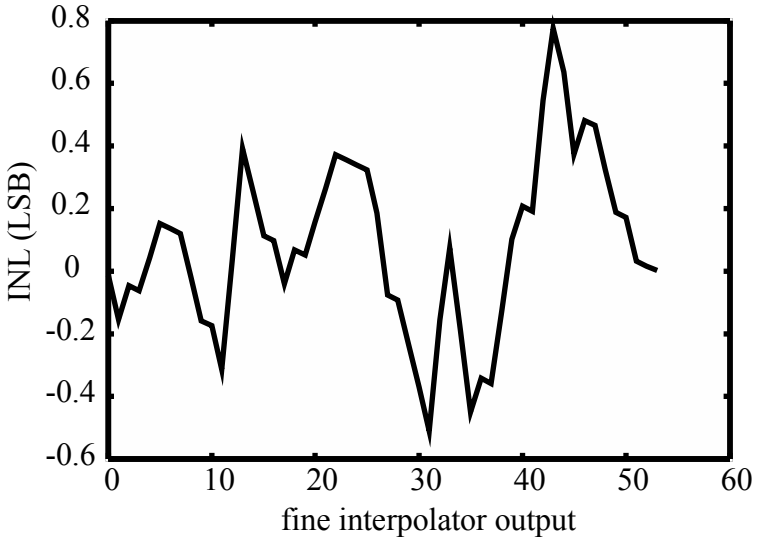
A first chip @ 180nm
Experimental Results



Resolution = 41 ps on 18 µs range

A first chip @ 180nm
Experimental Results

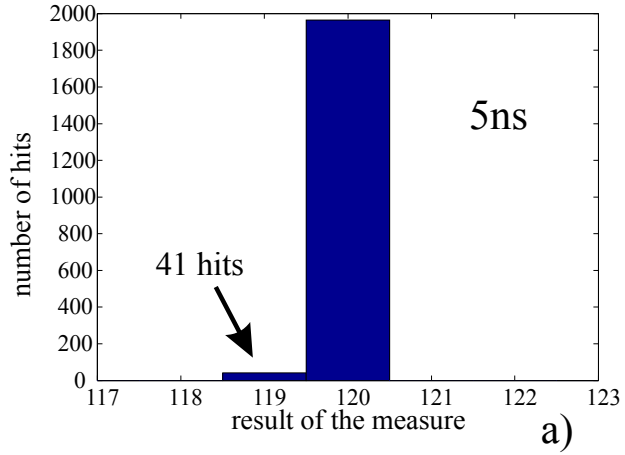


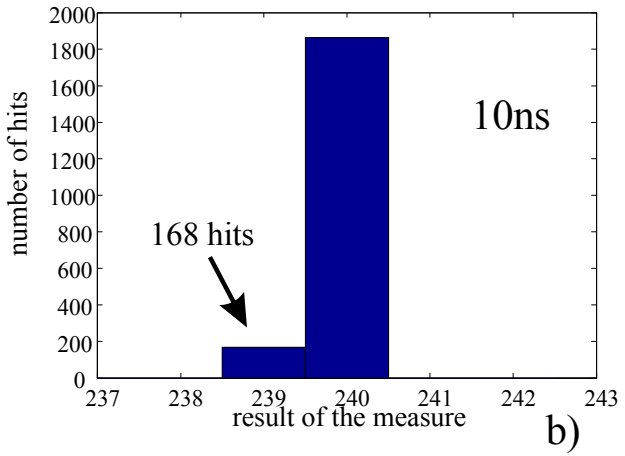


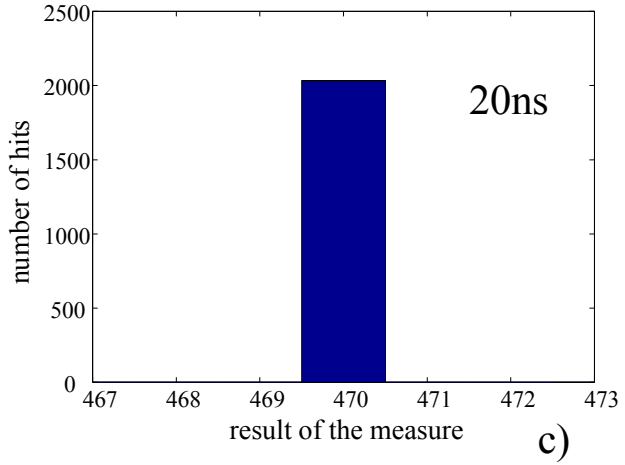
Max Differential Non Linearity
0.35 LSB

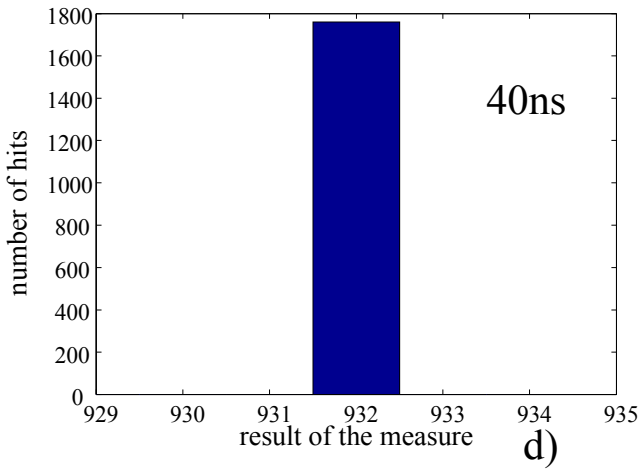
Max Integral Non Linearity
0.75 LSB

A first chip @ 180nm
Experimental Results



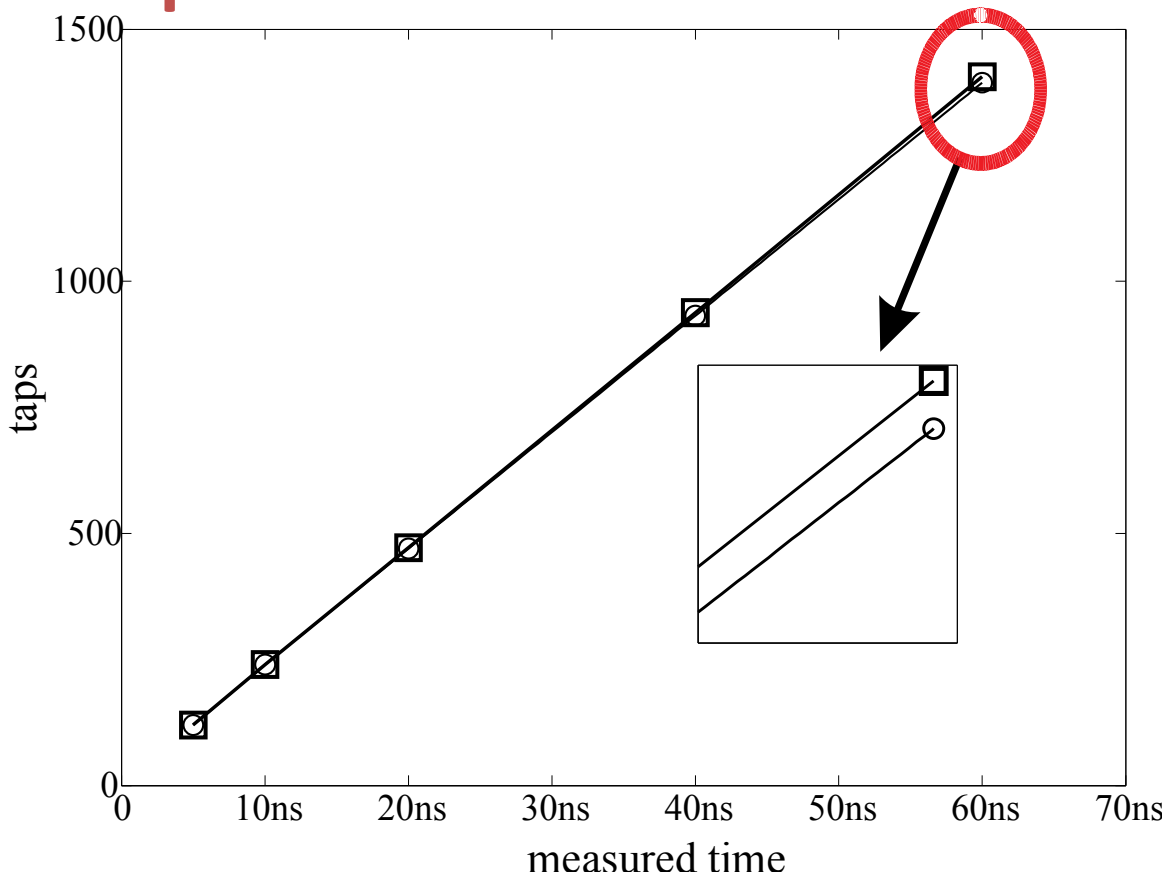






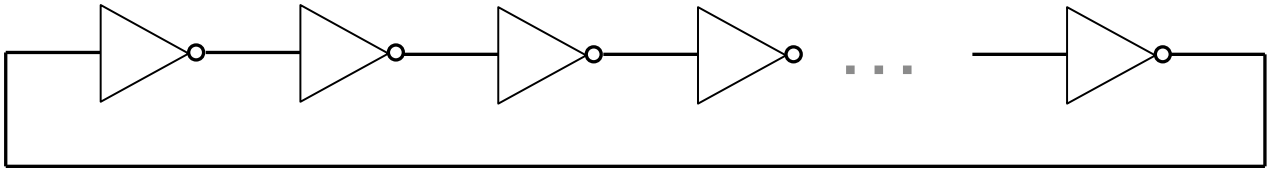
Single shot precision histograms

A first chip @ 180nm
Experimental Results

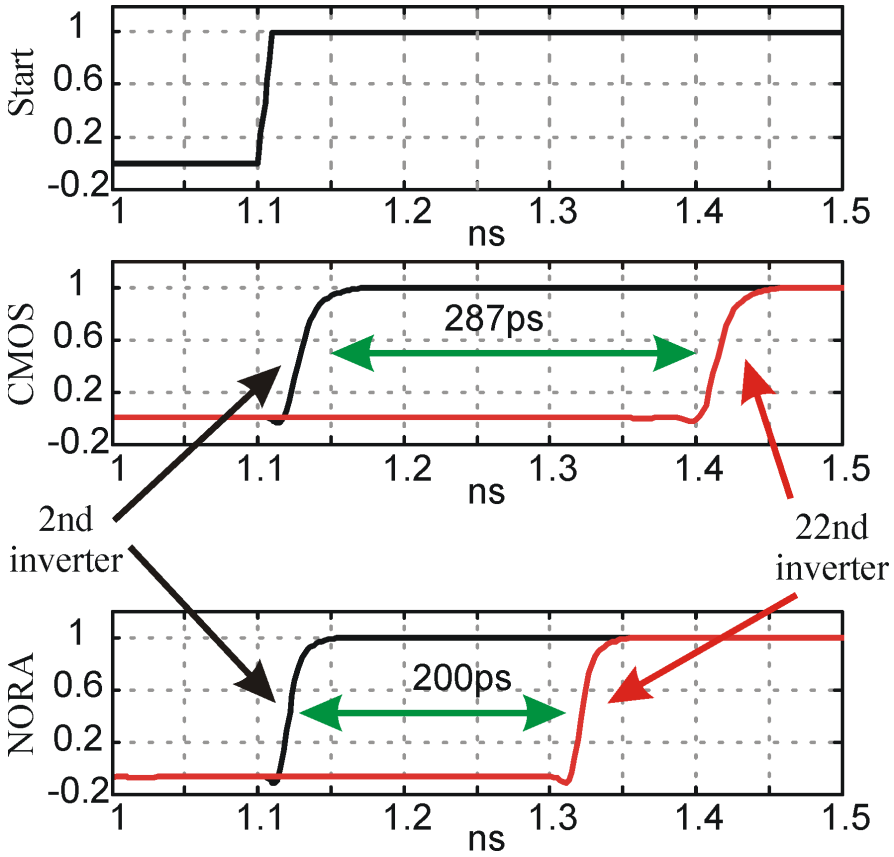


Single shot precision temperature dependence

NORA vs. CMOS @ 90nm

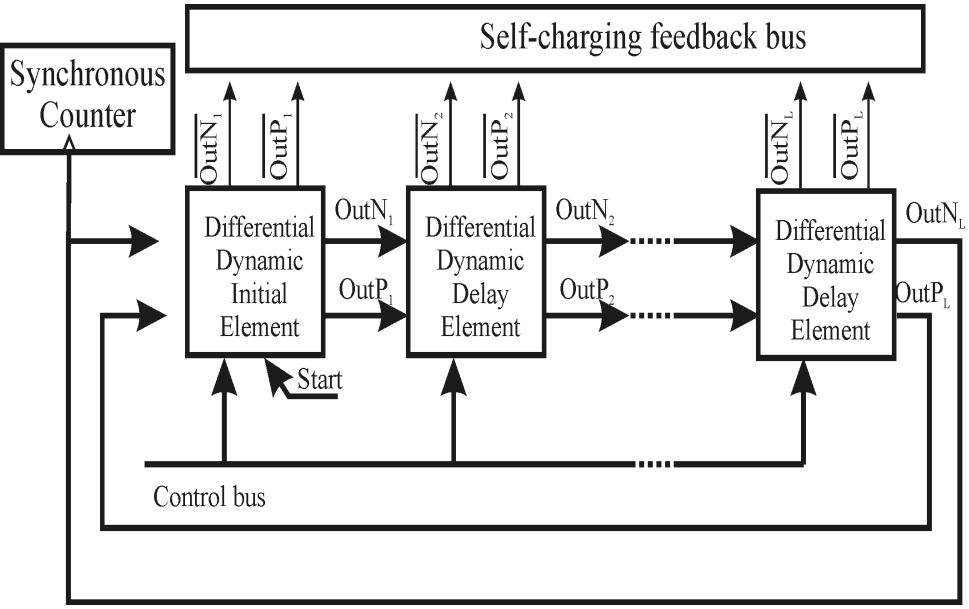


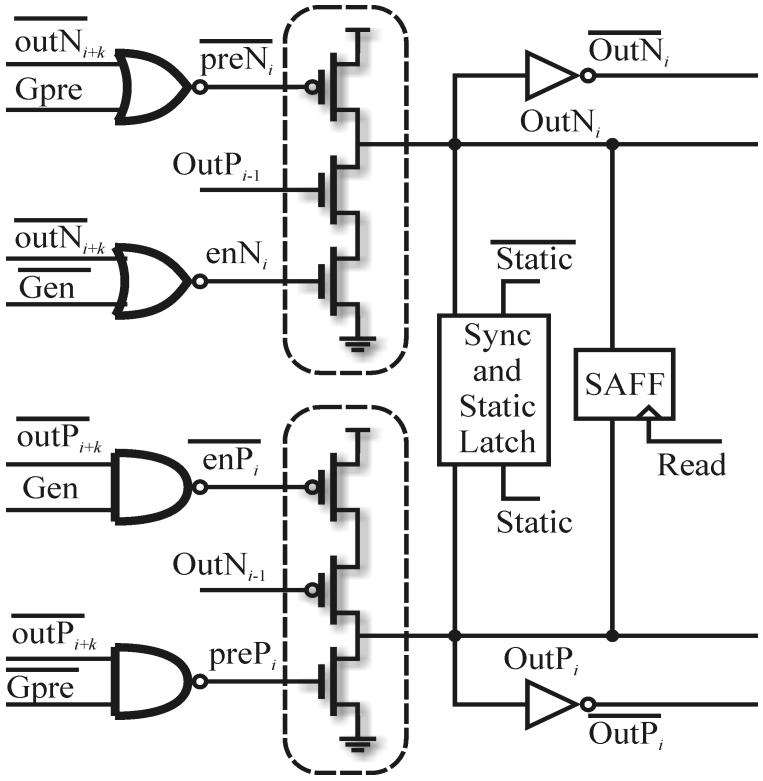
NORA is 29% Faster than CMOS



The TEMPO Differential scheme

The delay element compute two differential outputs.

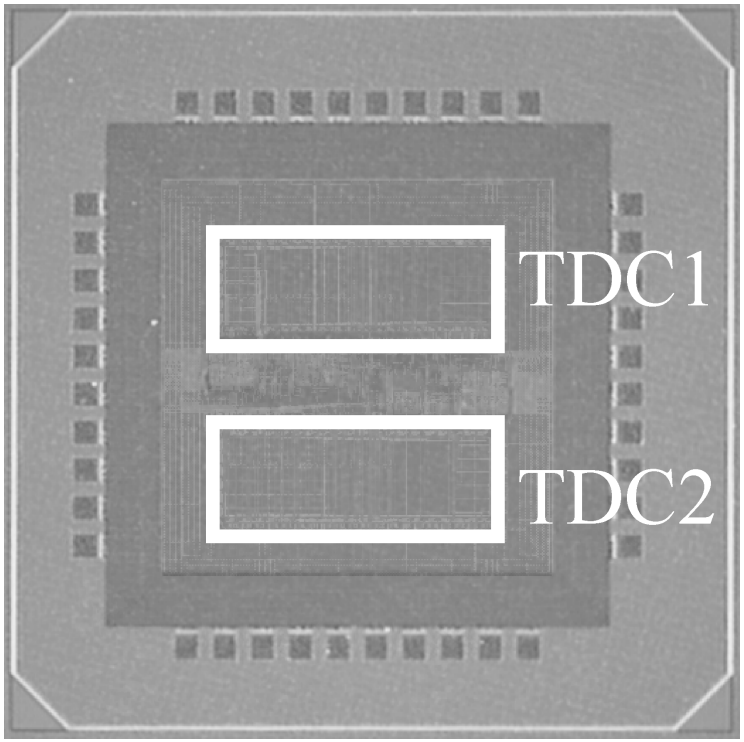




The output is stabilized by the latch and acquired by a Strong Arm FF

A second chip @ 90nm (UMC)

In the second chip the differential scheme was implemented



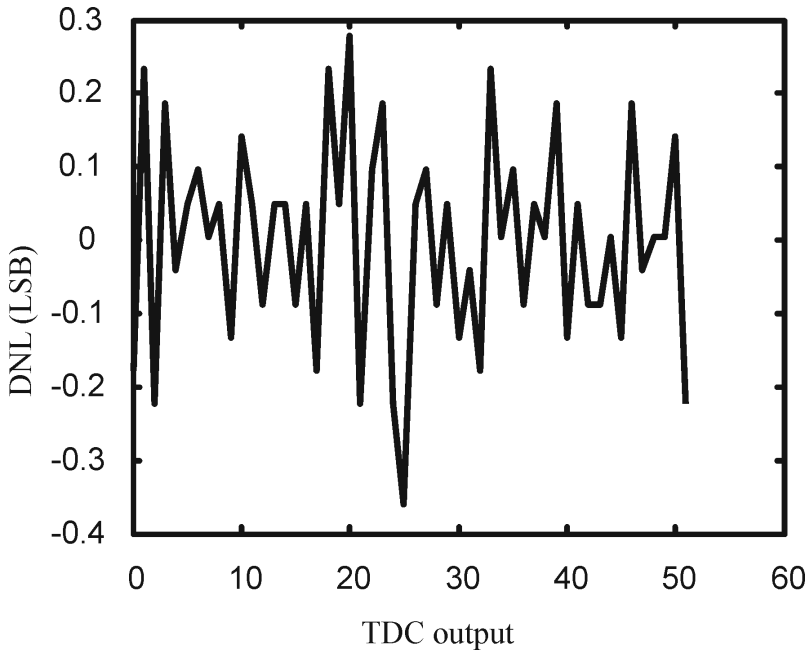
TDC1 measure the time between START & Stop

TDC2 measure a clock period (calibration)

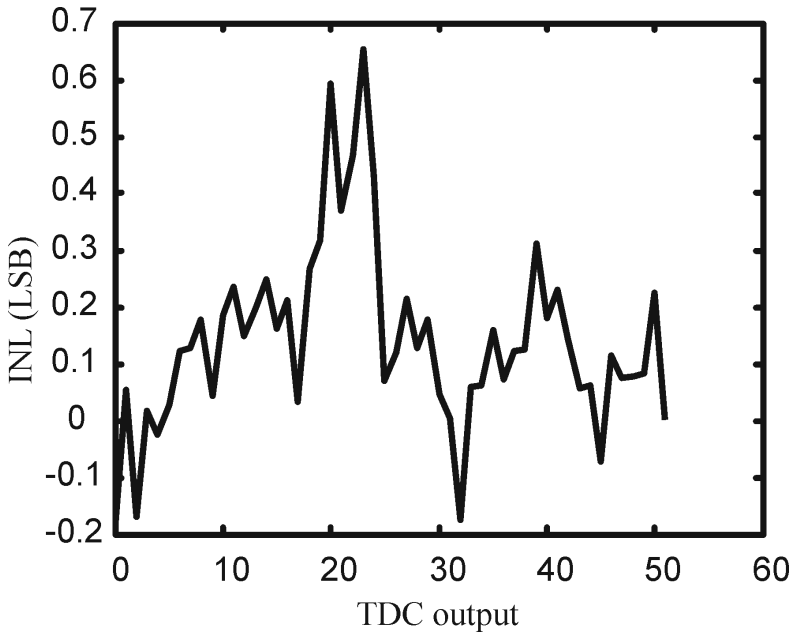
Full custom design for delay lines

Measured resolution 25 ps over 10.6 µs

A second chip @ 90nm
Experimental Results



Max Differential Non Linearity
0.35 LSB



Max Integral Non Linearity
0.65 LSB

Experimental Results Summary

Technology	Resolution	Range	Area	Power	INL	DNL
180nm	41ps	18µs	0.09mm	25mW	0.77LSB	0.35LSB
90nm	25ps	10.6µs	0.1mm	19mW	0.65LSB	0.35LSB