1 BaBar-Note 324. DIRC Electronics.

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Philippe Bailly (1), Christophe Beigbeder (2), Roger Bernier (2), Zhang Bo (1), Dominique Breton (2) Gérard Bonneaud (3), Robert Chase (2), Jacques Chauveau (1), Luigi Del Buono (1), Antoine Ducorps (2), Jean-Francois Genat (1), Aleksander Hrisoho (2), Hervé Lebbolo (1), Pierre Matricon (3), Christophe Renard (3), Gérard Oxoby (4), Sumit Sen (2), Christophe Thiébaux (3), Kai Truong (2), George Vasileiadis (3), Marc Verderi (3), Jaroslav Va'Vra (4), Guy Wormser (2).

Introduction

The DIRC electronics has been designed to match the requirements detailed in [1] in terms of timing and charge measurements from the Cherenkov photons generated in the quartz bars of the DIRC detector and converted by fast PhotoMultiplier Tubes (PMT) sensitive to single PhotoElectrons (PE).

These electronics are designed to fit the BaBar Front-end electronics and data acquisition standards [2] .

The Front-end electronics will be installed close to the detector in order to save cables and keep the required single photoelectron sensitivity. Therefore, it will be highly integrated, since it has to be housed in less than one cubic meter. In addition, dissipated power should be as low as possible; consequently, CMOS integrated electronics will be used wherever possible. It will be housed in 12 Front-end crates linked to the data acquisition system by BaBar standard 1.2 Gbit/s optical fibers. Twelve BaBar standard ReadOut Modules (ROM) process the DIRC raw data in parallel, for data-blocks building, detector calibration, and other purposes.

Solid state Light Emitting Devices (LED) illuminating the detector through the water are used for PMTs and Front-end electronics calibration.

High voltage is distributed using on-detector distribution boxes, the supplies being housed in six mainframes under control of the BaBar Environmental Control and Monitoring system.

(1) IN2P3, Laboratoire de Physique Nucléaire et des Hautes Energies. Universités Paris 6 et 7. T33 Rez de Chaussée, 75252, Paris CEDEX France.

(2) IN2P3, Laboratoire de l'Accélerateur Linéaire, Université Paris-Sud, Bat 200, 91245 Orsay CEDEX, France.

(3) IN2P3, Laboratoire de Physique Nucléaire et des Hautes Energies, Ecole Polytechnique, Route de Saclay, 91128 Palaiseau CEDEX, France.

(4) Stanford Linear Accelerator Center, Stanford University, PO Box 4349 MS 62 Stanford CA 94309 USA.

1 Electronics Requirements and Design Options

The electronics has to match the following requirements, as explained in [1], as it should not compromize the intrinsic detector performance.

- 1 The cost per electronic channel should be affordable.
- 2 Front-end electronics sensitivity: 15% of the mean single photoelectron response.
- 3 Electronics crosstalk less than 3%.
- 4 Electronics able to deal with a single-hit input rate of 100 kHz/channel.
- 4bis Electronics able to deal locally (e.g. 16 adjacent channels) fired at 10 kHz.
- 5,7,8 Best timing resolution compatible with technical and financial resources. The PMTs timing resolution, Time Transit Spread (TTS) around 1.5 ns, should not be degraded significantly.
- 6 Contribution to noise from the electronics should be negligible.
- 9 No amplitude readout is required on an event-by-event basis.
- 10 Amplitude readout should be available for monitoring and calibration purposes.
- 11 Sampled amplitude spectra should be available on real data.
- 12 Analog and digital test inputs have to be sent to the system for debugging purposes and in order to localize faulty components.
- 13 The ambient electronic noise should be maintained below 1mV.
- 14 A crate housing 1000 electronic channels should fit in a 35x50x50 cm3 volume.

- 1-1 Input Sensitivity

Threshold will be set at around 10% of the mean single PE response estimated to 20 mV at the input of the Front-end electronics. Consequently, the Front-end electronics has to allow a lowest threshold value of 2 mV at more, in order to let a safety margin of 0.5 mV w.r.t. requirement 2. Noise level (analog + digital) should be kept under 1 mV.

- 1-2 Time Precision

PMTs TTS is of the order of 1.5 ns rms [2]. The discriminators should have less than 1 ns spread over an amplitude range of 30. A TDC binning of 500 ps with integral and differential linearities below 0.5 LSB rms will match the requirements 5, 7, 8.

- 1-3 Calibration and Monitoring

In order to check the PMTs single photoelectron response, a calibration system sends 2ns wide blue LEDs light pulses, that will allow us to measure:

- The time offset and slopes of the TDC with respect to the machine frequency to better than 1 ns (requirements 5, 7, 8)

- Histograms of single PE responses will be built using charge measurements (requirements 10,11) fulfilling the following conditions:

  - Dynamic range: LSB = 8% of the threshold.

  - Full scale set to three times the single PE response.

  - Speed: Single PE histograms and threshold determination should be built within a few minutes (requirement 11). An eight-bit 35 MHz flash ADC shared by 64 channels will be used.

Provisions will be made to exercise the Front-end electronics with analog pulses similar to the PMTs pulses in order to localize faulty components using pseudo-gaussian pulses, of controlled amplitudes through a twelve-bit DAC, (requirement 12).

- 1-4 Readout and Processing Speed

The Front-end electronics will manage single input rates of 100 kHz, peak of 10 kHz on all channels, and trigger rates up to 2 KHz with 1 μs jitter (requirement 1). This requirement dictates a four-deep input channel buffer and associated readout hardware to keep deadtime due to channel buffer overload under 0.1% .

2 Overall System Description.

The overall DIRC electronics system and dataflow is shown in Fig. 1.

One DIRC Front-end Board (DFB) houses 64 photomultiplier channels. DFBs provide amplification, discrimination and shaping of the input current pulses, digitization of time and and buffering, digitization of charge and buffering for calibration purposes, selective buffering of data in time with the BaBar level 1 trigger, and response to readout requests from the BaBar data acquisition system. Charge is also sampled while data taking.

Fourteen DFBs are housed in each front-end crate, giving a total of 168 DFBs. Each crate is controlled by a DIRC Crate Controller (DCC) linked to DFBs through a Fast Protocol Distribution Board (PDB). Each DCC is linked to a ROM through a fast two-way optical link (Glink BaBar standard from Finisar and Hewlett-Packard, [4,5]) operated at 1.2 Gbit/s, connected to a personality interface card attached to the ROM. Glink is made of two independent unidirectional fibers: The Control link (CLINK) to the detector for control, and the Data link (DLINK) from the detector for data return [3]. ROMs are housed in a single VME readout crate (BaBar standard)

Twelve ROMs are controlled by a Read Out Controller (ROC BaBar standard) in the VME DAQ crate. As for other detectors, fast controls are originated in the Fast Control Distribution Module (FCDM, BaBar standard), in the VME readout crate, and sent to the ROM via the Fast Protocol Distribution Board (PDB) Clock rates at the DFB input are derived from the machine frequency (476 MHz). Each DCC sequences the serial data flow bit by bit to the 16 stations of the Front-end crate. Therefore, the clock rate at the DFB input is chosen at 476/8 = 59.5 MHz, since the Glink is operated at 1.2 Gbit/s (the serial protocol inserts start and stop flags between data words). This 59.5 MHz frequency is used as a time reference by the TDCs, and divided as sub-multiples for internal DFB management.

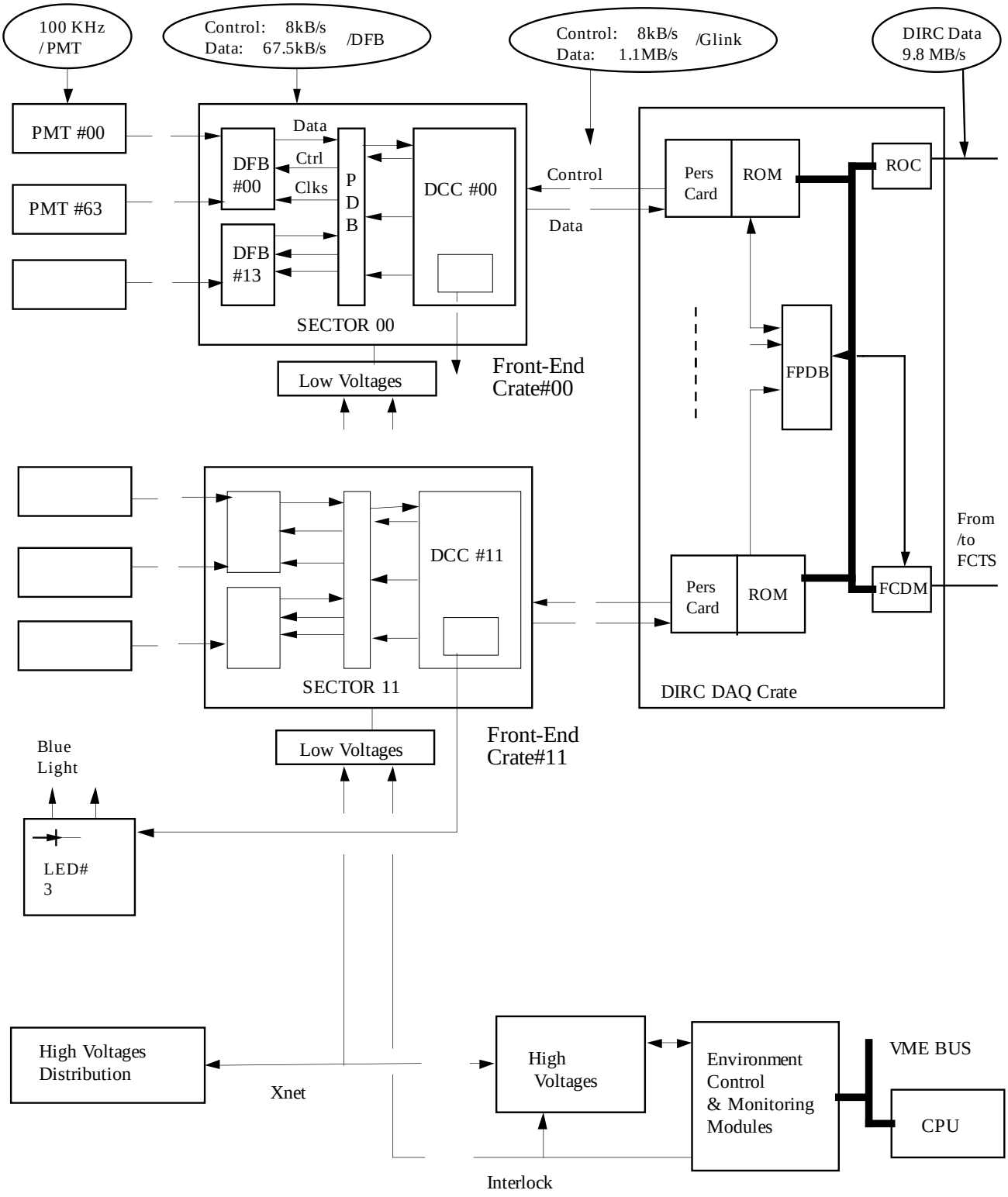

Figure 1: Dirc Electronics Overall Block Diagram and dataflows.

3 Readout and Control Dataflows

The required input rate is 100 kHz per PMT channel at 10 times nominal background. The L1 trigger rate is 2 kHz [7], with 11.5 μs latency and 1 μs resolution. Actually, the DFB is able to endorse a rate up to 10 kHz. Taking into account the data packets format [3], the average dataflow at the output of the DFBs is 67.2 kByte/s. At the output of the DCC, on the Glink data channel, it is 1.1 MByte/s, far from the Glink capability, and 9.8 MByte/s at the DIRC readout crate output. The control flow seen at the DFB input is only 8 kByte/s, identical to the Glink control channel.

During calibration runs where all the channels (or half) are pulsed at the same time, it should be possible to tune the pulse frequency and readout rate to make the dataflow approach the maximum Glink throughput, in order to reduce the total calibration time.

4 Analog Chip

The analog chip [8] block diagram is shown in Fig. 2. It processes the input PMT pulse in two independent ways:

- 4-1 Zero-Crossing Discrimination.

A time resolution better than 800 ps over an amplitude range of 30 is achieved using the zero-crossing of the differentiated input pulse. Actually, an hysteresis comparator is set when the differentiated input crosses a threshold of a few negative millivolts. The hysteresis is equal to the threshold, therefore the discriminator is reset when a zero level is crossed. This trailing edge, in time with the zero-crossing is differentiated to provide an output pulse of a few nanosecond. The effective threshold is obtained moving the input amplifier gain, corresponding to an input threshold between 1 and 10 mV. The dead time after a zero crossing is 80 nanosecond.

- 4-2 Pseudo Gaussian Pulse Shaping

A CR-RC pulse shaper peaking at 80 ns provides a maximum output proportional to the input charge, used for charge measurements in calibration modes. Analog voltage gain is between 2.5 to 25 through this channel. Further amplification by a factor of five is needed to match the ADC sensitivity.

The analog chip is manufactured by AMS (Austria Mikro Systems) using a 1.2 micron double-poly / double-metal CMOS process. It is intended to integrate eight channels, limited by the overall power manageable within a chip: 0.4 W in total, and the available packages in terms of I/O pins count.

5 Digital Chip.

The digital chip is described [9a,b,c]; Fig. 3 shows the bloc diagram. The main features following the requirements [1] are:

- 16 TDC channels.
- 500 ps binning.

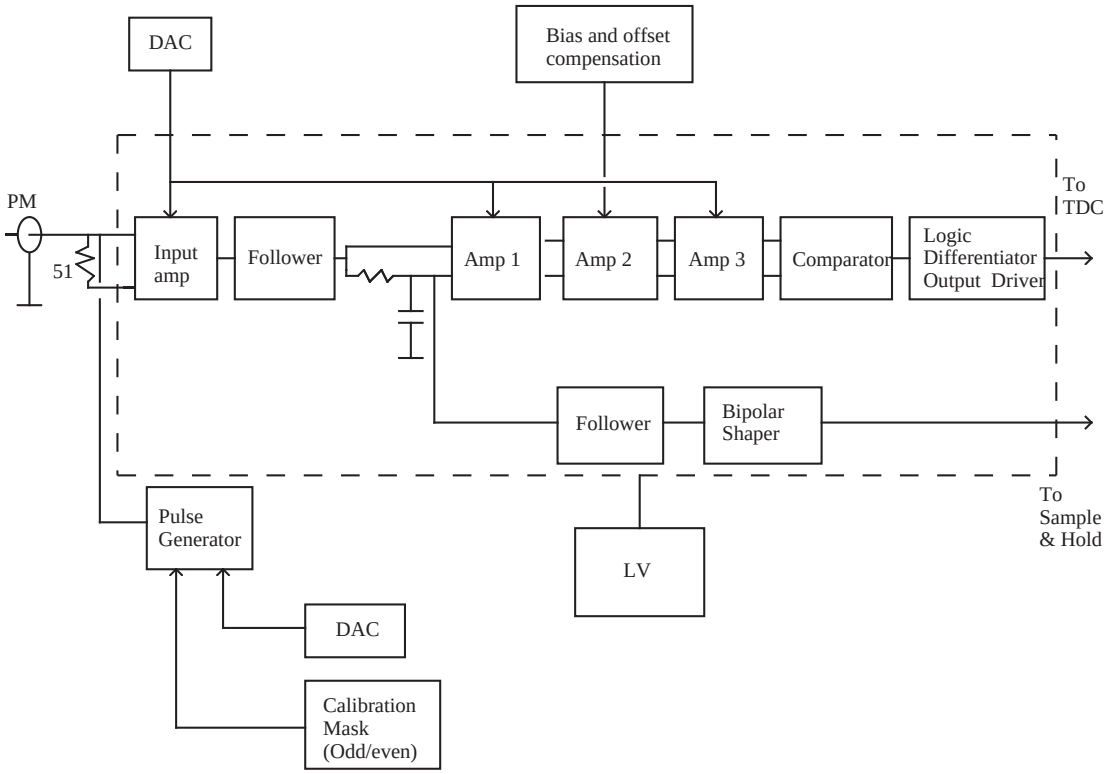

Figure 2: Zero Crossing Discriminator and Shaper.

- 32 μs full scale.
- 32 ns double-hit resolution.
- 59.5 MHz reference clock.
- 4 word-deep channel FIFO buffers.
- Simultaneous Read and Write operations.
- Maximum input capability:
  - average: 500 KHz on any of the 16 channels.
  - peak on one single channel: 4 hits within 1 us.
  - peak on 16 channels: 96 hits within 3 microseconds.
- Selection of data within a programmable time window is available at any time for readout. the window size can be set between 64 ns and 1.984μs (5 bit) and the latency between 64 ns and 16.284 μs (8 bits).
- Selective readout can be disabled (readout of any data).
- A bit pattern of the FIFO overloaded during the trigger window (i.e processed as the selective readout of time data) is available as an End Of Block.
- Channel disabling selectable between 500 kHz and 8 MHz single channel input rate.

Within a 59.5 MHz input clock period, a fine time measurement on 5 bits is achieved using voltage-controlled digital delay lines synchronized on the clock period using a calibration channel generating a reference voltage, to compensate for temperature, supplies, and process delay variations. This calibration is fully transparent.

A synchronous counter covers the 11 higher order bits.

In order to allow data-driven operations and asynchronous readout occuring at any trigger time during BaBar runs, three levels of FIFO memories allow to write input data from the TDC section, and simultaneously read output data associated to an incoming trigger.

The input FIFOs of depth 4 store data just coming out from TDC encoding, for at more 1 μs, before transfer to a latency FIFO of depth 32. Data are kept there for the minimum trigger latency, before transfer to the output FIFO, staying for the trigger resolution, waiting for an incoming L1. Both trigger latency and trigger resolution are programmable. Therefore, an incoming readout request gets only data falling within the programmed time window, allowing a factor of ten less data to be read, under the current BaBar trigger timing (latency 12 μs, resolution 1 μs, [7]). Noisy channels can be dynamically disabled if the input rate exceeds a programmable limit that can be set between 500 KHz, and 8 MHz. Each FIFO overload or channel disabling during a trigger window is reported at the end of each data block in a sixteen bit pattern. A maximum average channel input rate of 600 KHz is accepted, as far as there are less than 4 input hits on the same channel within a window of one microsecond, and less than 96 on any of the 16 channels within one trigger latency.

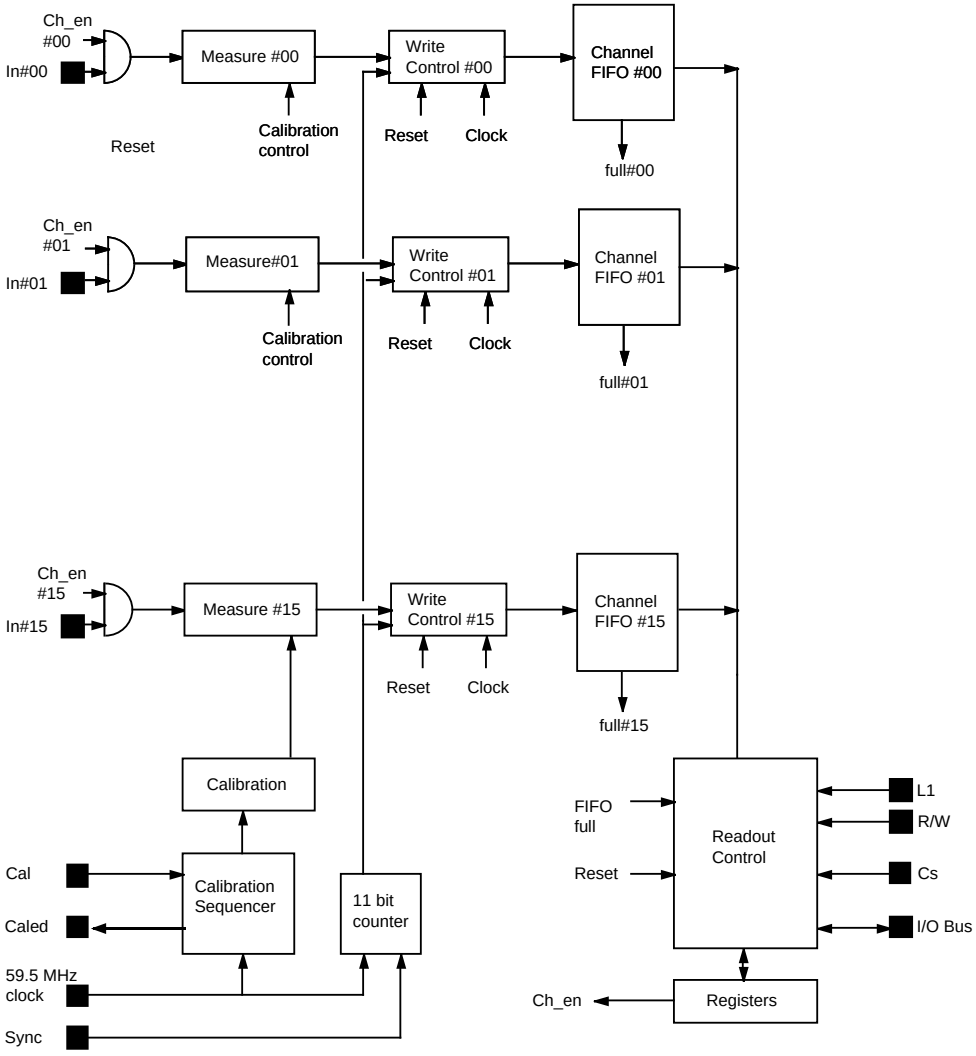

Figure 3: Digital Chip Block Diagram.

The digital chip is manufactured by ES2, using a 0.8 microns Dual Metal CMOS process. Power dissipation is less than 100 mW at 100 kHz input rate.

6 Charge Readout

There is no need for charge readout on an event-by-event basis. However, it is mandatory to understand the behavior of the photomultipliers from single photoelectron spectra. Consequently, four modes of charge readout are foreseen, using an eight-bit ADC shared by the 64 channels of a DFB. An analog multiplexer selects the proper channel to be digitized according to the charge readout mode.

- 6-1 Discriminator Triggered Mode or Strobed Mode

Either the discriminator output or the properly delayed Calibration Strobe sent through the CLINK triggers the Flash ADC. A bit on a DFB control register selects the mode.

- 6-2 Addressed or Multiplexed Mode

Either the ADC is addressed towards a given channel selected on the DFB through a local command, or towards the first channel that has been fired, using a priority logic with the ADC being ready for the next hit after the conversion time. A bit on the DFB control register selects the mode.

Depending on whether the calibration LEDs illuminate the concerned channel, noise pedestal or photoelectron signals are digitized.

Any combination of these modes allow to build histograms of the phototubes and associated analog electronics response for all DIRC channels.

7 DIRC Front-end Boards (DFB)

The DIRC Front-end Digitizers Board data path is shown in Fig. 4.

DFBs [14] house:

- Eight analog chips,
- Four digital chips,
- One eight-bit 35 MHz ADC,
- Four threshold DACs
- Four Multi-Event buffers of 2K 32-bit words,
- A few Programmable Logic Devices integrating sequencers and protocol decoders,
- Two calibration generators (odd/even channels) associated with one 12-bit DAC.

The DFBs respond to the DIRC commands as detailed in [6]. These commands are grouped in two sets:

- Global commands, managing the broadcast fast controls such as synchronization, counter clears, trigger, readout, calibration. Associated data such as trigger tag, are dispatched with these commands.

- Local commands, such as registers access, calibration modes and levels, and test controls.

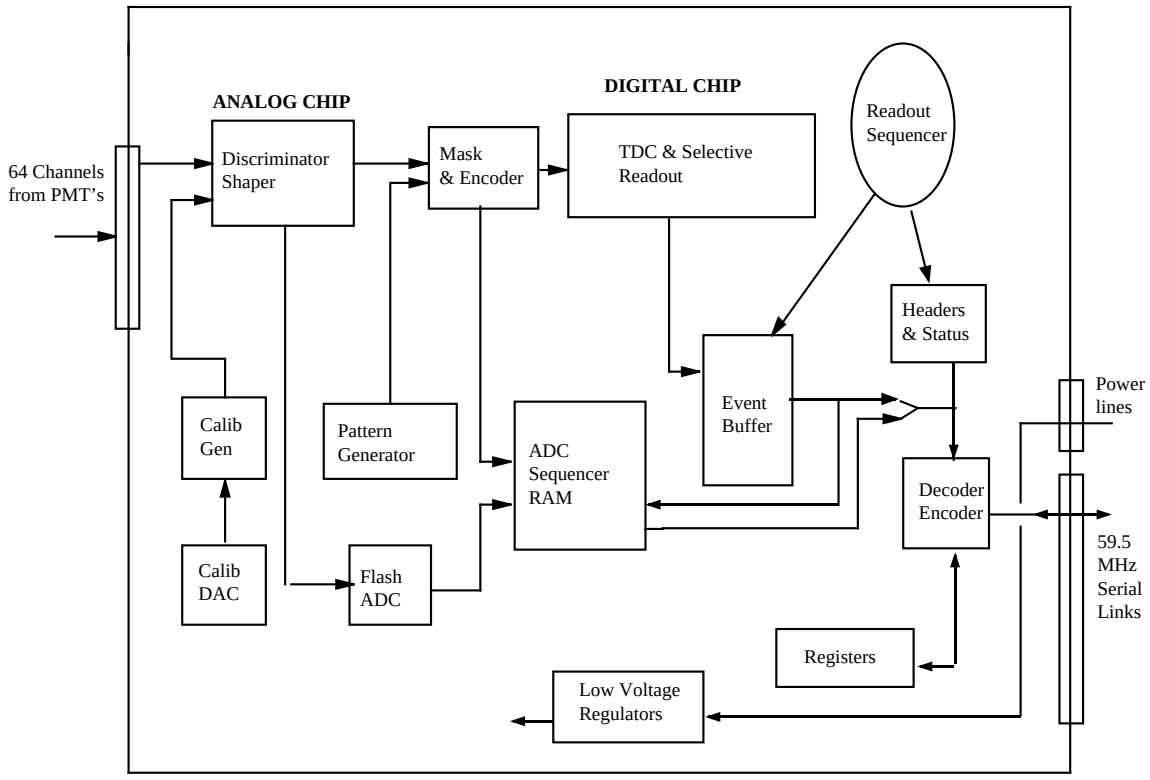

Figure 4: DIRC Front-end Board data path

Data stay on the DFBs for the L1 trigger latency. On receipt of the L1 trigger, data are output in parallel from the digital chips to four Multi-Event Buffers of four-event depth, where they stay until receipt of a readout strobe. Input FIFO buffers integrated in the Digital chips ensure that deadtime is less than 0.1 % under 100 kHz average input rate. The charge readout is enabled according to the modes described above. Data are packed in blocks including headers and trailers, reflecting eventually the overload of input FIFOs.

8 DIRC Crate Controller

The DIRC Crate Controllers [12] shown in Fig. 5, housed in the Front-end crates, demultiplex the 1.2 Gbit/s serial data on the Glink to 59.5 Mbit/s at the DFB input.

Slow controls such as low voltage and temperature monitoring are managed by a eigth-bit microcontroller linked to the Environmental Control and Monitoring Crate (ECMC). ECMC [20] keeps track of temperature, currents, voltages, calibration constants, detector environmment parameters associated to data.

A low-jitter Phase Locked Loop device will eventually recover the 59.5 MHz frequency with phase jitter within 150 ps RMS, if significant phase jitter in presence of data is found at the HP chips clock recovery output. Lower frequencies are generated for other clocks to be dispatched to the DFBs.

A fast pulse is also generated on Calibration Strobe receipt [16], to feed each of the 12 blue LEDs used for the detector calibration. The pulse is programmable in delay by steps of .

Preliminary measurements show that the recovered clock jitter at the output of the HP chip (with no data transmitted), is less than 200 ps rms.

9 Protocol Distribution Board (PDB).

Signal dispatching is achieved using a Fast Protocol Distribution printed circuit Board (PDB), feeding clocks and data to each of up to 14 DFBs. The PDB has four sets of 14 lines for control, control clocks, data clocks and data lines. Two versions are currently under development: a multiwired prototype, and a printed circuit using strip lines are investigated in terms of transmission line media at 59.5 MHz, over 40cm long distances. Both implementations give good signal transmission up to 100 MHz [10].

10 Readout Modules and Personality Cards

These modules are similar for SVT, DIRC, and IFR BaBar sub-detectors.

The DIRC Front-end is read by twelve DAQ Readout Modules [11], each connected to a Glink interface housed on a detector dependent Personality Card. The DAQ Readout Module and Personality card are housed in a VME crate (DAQ Crate) controlled by a ReadOut Controller (ROC), linked to the BaBar Data Acquisition system by a serial interface.

The DIRC Personality card [13], part of the ROM shown in Fig 6, is a link controller, feeding data from the Front-end to the Video RAM (DLINK) in the ROM under control of a state machine, and decoding control from the FCDM in the DAQ crate down to the Front-end (CLINK).

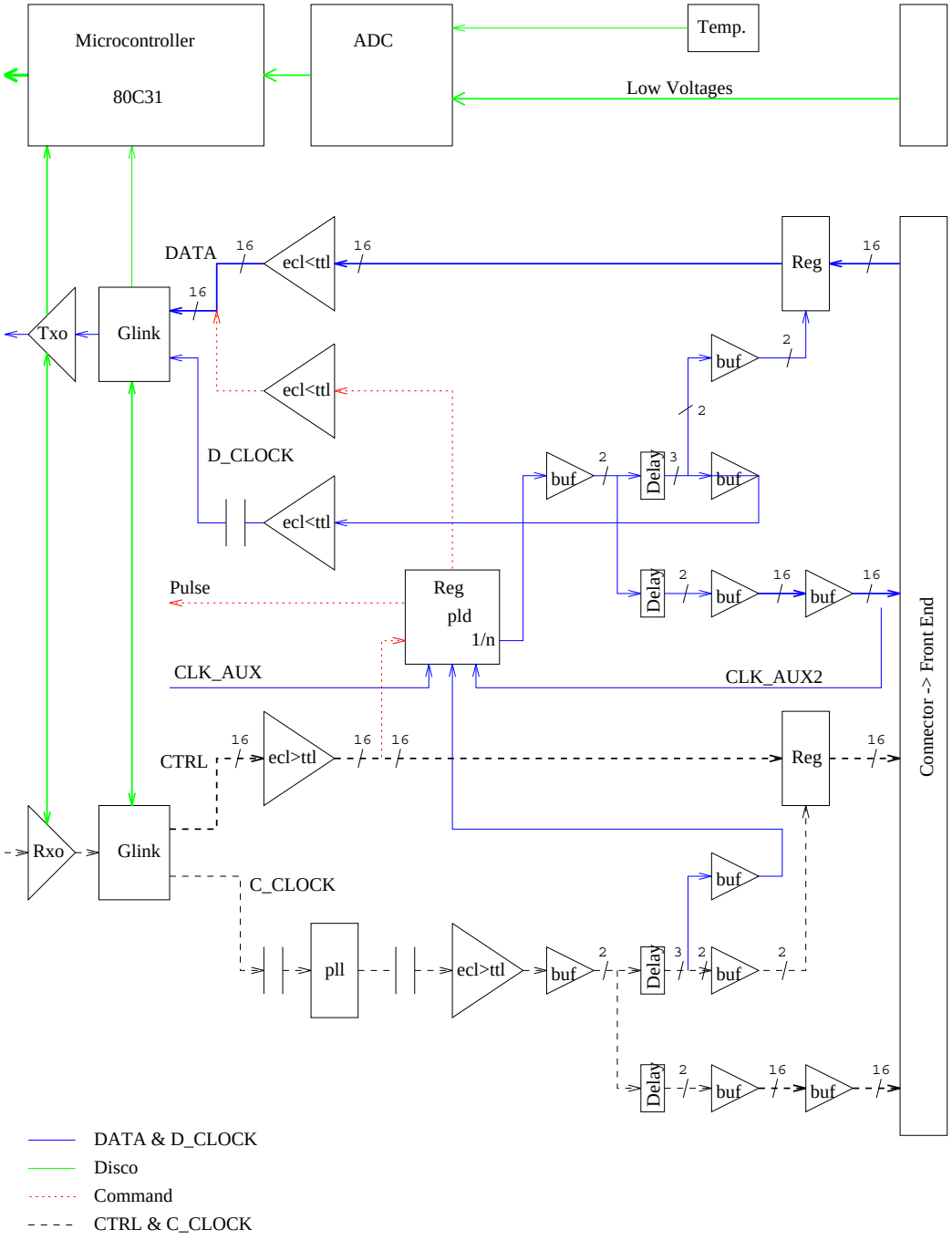

Figure 5: The DIRC Crate Controller.

The Fiber optics is interfaced using standard Receiver-Transmitter and Optical Interface chips. Logic is integrated in a ORCA Programmable Logic Device. A VHDL description is used for modeling/programming the device.

11 Grounding and Shielding

Grounding and Shielding of the DIRC Electronics is described in [15]. A flexible scheme allowing to connect or not the signal ground (PMT base ground) of each channel to the Standoff-box has been chosen. The 50 Ohms coaxial braids are grounded on both sides, to the signal ground on the PMT base side, to the DFB unique ground plane on the other side. The analog chip is connected to the signal on the non inverting input, the calibration signal common to all odd or even channels on the inverting input.

The HV cables ground is connected through a 100 Ohms resistor (that can be shunted) on the PMT base. Front end crates are grounded using one braid per crate, connected to one unique grounding point on the Standoff-box.

This scheme provides a good high frequency pick-up rejection, depending whether the Standoff-box can be taken as a clean ground, the individual ground connection of the PMT bases will be used or not.

12 Calibration

Electrical calibration is achieved using a pseudo-Gaussian shaped signal of amplitude controllable with a 12-bit DAC. A calibration mask odd/even channels or both is used, to estimate the first-order inter-channel crosstalk.

Time calibration (t0 and slope) will be achieved using the calibration data calculated from the DFBs response from the short blue LED light pulses (2ns) sent to the full detector [15]. Sub-nanosecond precision will be obtained from multiple pulsings, within a few minutes.

13 DIRC commands

DIRC commands [6] are either global to BaBar or local (DIRC only).

- 13-1 Global Commands

- Clear: Resets input FIFOs and Multi-Event Buffers.
- Sync: Clears all counters.
- L1: Initiates Digital-Chips output FIFO to Multi-Event Buffer transfers. Trigger tag is sent as data.
- Readout strobe: Initiates Multi-Event Buffers readout.

- 13-2 Local Commands

-13-2-1 Readout setup:

- Threshold DACs.
- Channel select for charge measurement.

Figure 6: Readout Module Block Diagram

- Channel Enable pattern.
- Trigger Latency and Resolution.
- Local Reset.

-13-2-2 Calibration:

- Calibration mode.
- Odd/Even channels to be pulsed (2 bit).
- Signal origin: LED pulse or DAC pulse (1 bit).
- Strobed or data driven readout (1 bit).
- Channel or dynamic selection for charge readout (1 bit).
- Calibration DAC (12 bit).
- LED timing (to DCC) (6 bit), LED duration, LED amplitude , LED frequency .

14 Test Benches

- 14-1 Test Benches at LAL Orsay

Test benches are currently in use, or under design at LAL for checking:

- The analog chip prototypes on a dedicated test bench,
- The analog chip prototypes on the DFBs,
- The analog chip production with an automated software driven tool,
- A test bench of the DFB versions
- A test bench of DCC and DFBs running together

- 13-2 Test Benches at Ecole Polytechnique

The test bench at Ecole Polytechnique is dedicated to the DCC and the PDB checks. It is designed for data transmission tests up to at least 59.5 MHz rates and will be used to set up the slow control part of the DCC. This test bench uses VME and the real time operating system VxWorks to make it able to evolve towards a standard BaBar like environment.
par the components of this test bench are:

- VME crates;
- The VxWorks part which comprises:
  - One MVME167 module housing a 68040 Motorola CPU running under VxWorks. It is the crate controller. A MVME712M transition module is used to connect the CPU to the network and will be used to access the DCC μ-controller.
  - One HP-J200 which is the VxWorks UNIX host.
  - X-terminals to log on the MVME 167 via remote login.

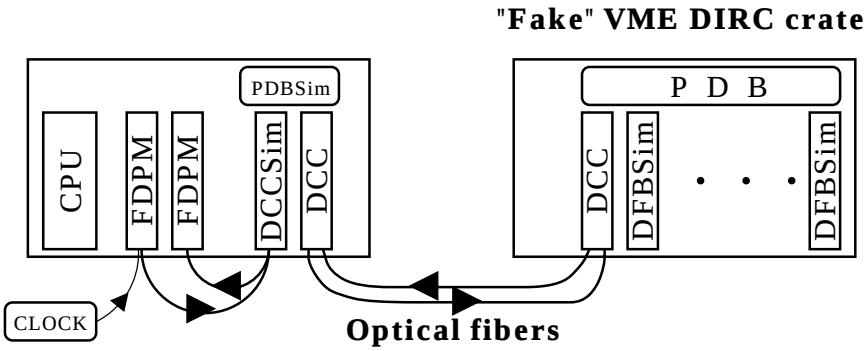

Figure 7: Test chain faking a DIRC crate.

- Two Fast Dual Port Memory cards (FDPM) [17] from CERN, providing the high speed part of the test bench. These modules can send/record up to 128k of 8, 16, 24, or 32 parallel bit patterns up to 100 MHz.
- Devices designed at Ecole Polytechnique:
  - DCCSim: it is an interface between the FDPMs and the PDB. It provides 2*16 clocks distribution and 2*16 Data/Control link accesses on the PDB, as for the DCC.
  - DFBSims: they copy the data from from the Commands-links to the Data-links of the PDB to fake the presence of a DFB receiving/sending data.
  - PDBSim: it allows a connection through the P2 connector between a DCCSim and a DCC.
- Additional devices: scopes, pulsers, supplies and others.

The major tests are:

- PDB alone:
  - PDB characteristics: bandwidth, characteristic impedance and others,
  - Test of data transmission through a PDB.
- DCC alone:
  - Glink synchronization,
  - Measurement of the recovered clock jitter,
  - Test of data transmission looping through the optical fiber.
- DCC + PDB: Test of data transmission looping through a chain faking a DIRC crate as shown Fig 7.
- Slow control part of the DCC.

Future tests using real DFB are foreseen.

- 13-3 Test Benches at LBNL

A proposed test bench at LBNL [18] to be progressively implemented for the full DIRC electronics tests, makes use of:

- SUN station,
- VME crate and readout,
- DAQ card prototype equipped with a Personality Module,
- Prototype DFB equipped with analog and digital chips,
- Pulser, signal generator and NIM logic,
- Basic ADC and TDC.

The first tests would use both on-board and external pulsing in order to debug both hardware and software. These tests would check:

- Register access,
- DFB calibration,
- DFB readout section functionality using pulses at the digital chip input, and L1s,
- GLINK and DCC with PDB,
- Recovered clock stability at the GLINK output in presence of data,
- Analog measurements, TDC operations and selective readout, full calibrations.

Further tests with photon signals would require in addition:

- At least one DIRC Front-end crate,
- At least one PDB card,
- At least one DCC,
- A dark box and PMTs,
- LED and pulsing circuits,
- 2d generation DFB prototype cards,
- Fast control modules.

These last tests would check:

- Several DFBs running together with DCC and PDB.
- Real signals from PMTs using the dark box and the pulser.
- Architectural tests with several Front-end crates, and as many ROMs as crates.

- 13-4 Test benches at LPNHE Paris

A test bench is under implementation at LPNHE Paris for testing the production of the digital chips. It is an extension of the test benches used to test the two first prototypes. For each, a multilayer test card has been designed. These cards have been interfaced to a MacIntosh computer running LabView, under control of a dedicated software. The test benches were equipped with a clock generator, a LeCroy 9210 precision pulser (10 picosecond LSB), low power supplies, and a digital I/O card. The automated tests will make use of a hardwired sequencer on the test card producing digital patterns and bursts of input pulses.

14 High Voltage System

The High Voltage distribution scheme [19] [20] makes use of one HV channel for 16 PMTs, giving a total of 56 HV channels per sector. Taking into account that each PMT base needs a maximum value of 0.3 mA at 2 kV, each HV channel will be able to deliver a maximum current of 4.8 mA at this voltage.

The current design is based on HV modules that provide 12 HV channels/module, giving a total of 5 HV modules per sector (4 spares channels are available per sector). The 10 HV modules needed for two sectors are housed in one High Voltage mainframe crate, giving a total of only 6 mainframes for the whole DIRC High Voltage system. Finally, only one multiconductor coaxial cable per sector will provide the High Voltage to the PMTs.

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